Compal LA-H151P

Capela Windows Schematic Document

AMD Stoney Ridge FT4

REV :1.0

2018-12-03

Security Classification	Compal Secret Data		
Issued Date	2018/03/12	Deciphered Date	2019/03/12

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Title: Cover Page

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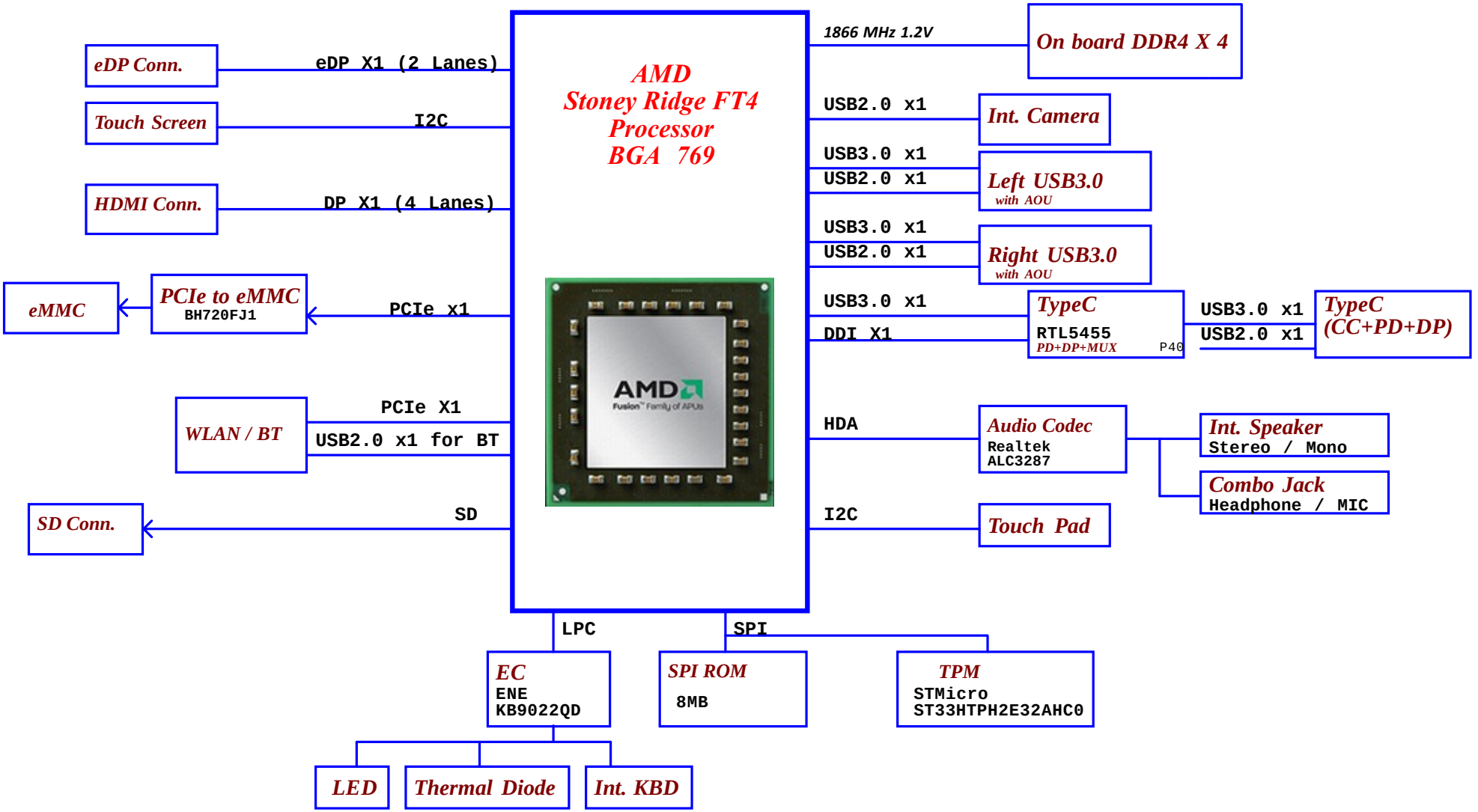
AMD Stoney Ridge FT4



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Title: Block Diagram

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Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
+12.6VB	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+0.95VALW	0.95V always on power rail	ON	ON	ON
+0.95VS	0.95V switched power rail	ON	OFF	OFF
+1.2V	1.2V power rail for APU and DDR	ON	ON	OFF
+2.5V	2.5V switched power rail for DDR	ON	ON	OFF
+0.6V	0.6V switched power rail for DDR terminator	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTCVBATT	RTC power	ON	ON	ON

SMBUS Control Table

	SOURCE	APU	BATT	NPCE388N	SO-DIMM	WLAN	RTS5455
EC_SMB_CK1 EC_SMB_DA1	ENE9022 +3VL	X	V +3VALW	X	X	X	X
APU_SCLK0 APU_SDATA0	APU +3VS	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	ENE9022 +3VS	V +1.8VS	X	X	X	X	V +3VALW

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011x b	16H
Charger	0001 0010 b	12H

EC SM Bus2 address

Device	Address	HEX
APU	1001 100X b	98H
RTS5455	1010 1100	

APU PCIE PORT LIST

Port	Device
0	SSD
1	
2	WLAN
3	eMMC

USB Port Table

USB 3.0	USB 2.0	3 External USB Port
	0	
	1	WLAN/BT Combo
	2	Camera
	3	
0	4	TYPEC
1	5	Left USB3.0 port
2	6	Right USB3.0 port
	7	

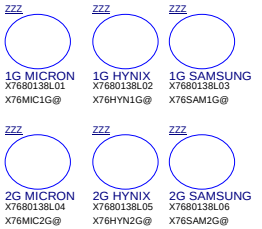
USB OC MAPPING

OC#	USB Port	
0	USB2 port5	
1	USB2 port6	
2		
3		

DDR SDP/DDP STUFF OPTIONS

Part	SDP	DDP
RD35-38	0HM	240HM
RD39	N/A	STUFF
RD57	N/A	STUFF
RD56	STUFF	N/A

DDR X76



PCB

ZZZ
DAZ2G500100
PCB ELAC2 LA-H151P LS-H151P 02

APU part

X4E EMC

STATE \ SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF

BOM Structure Table

BOM Structure	Item
@	Unpop
HDT@	AMD Dubeg Header
TPM@	TPM part
EMMC@	EMMC part
X76@	X76 level BOM
EMI@	EMI pop component
@EMI@	EMI Un pop component
ESD@	ESD pop component
@ESD@	ESD Un pop component
RF@	RF pop component
@RF@	RF Un pop component
ME@	ME part
SDP@	On board DDR SDP part
DDP@	On board DDR DDP part
TYPEC@	TYPEC part
KBL@	Keyboard backlight part
NONTPM@	NONTPM part for STRAP pin

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Title: NOTES LIST

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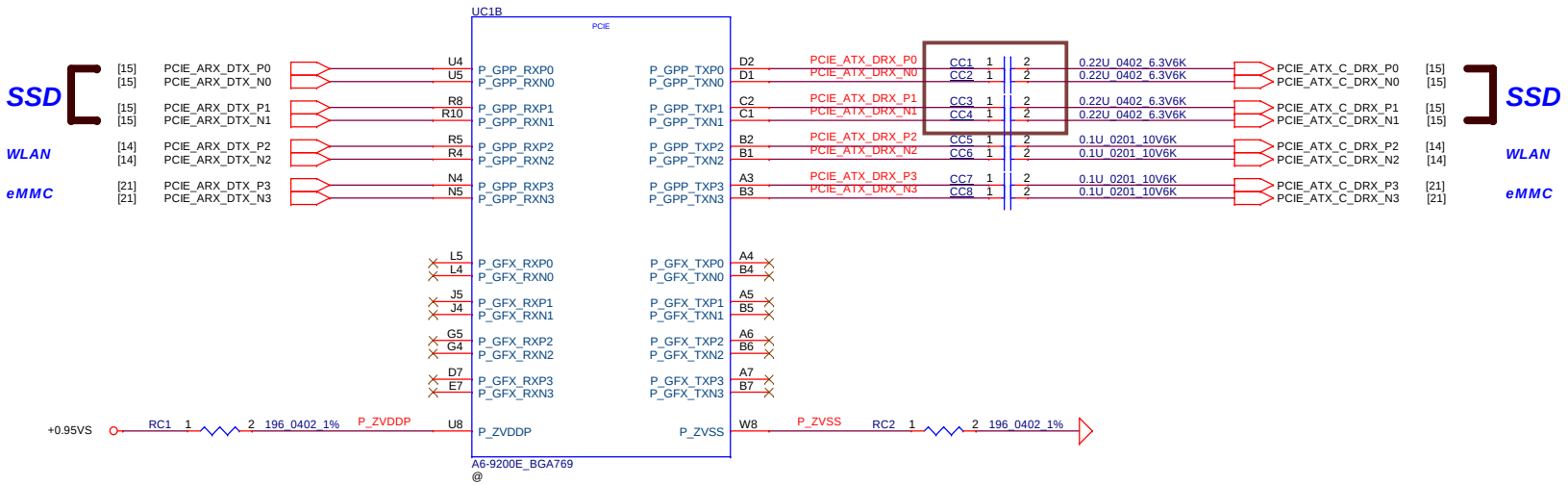

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Title: GPP & PCIE

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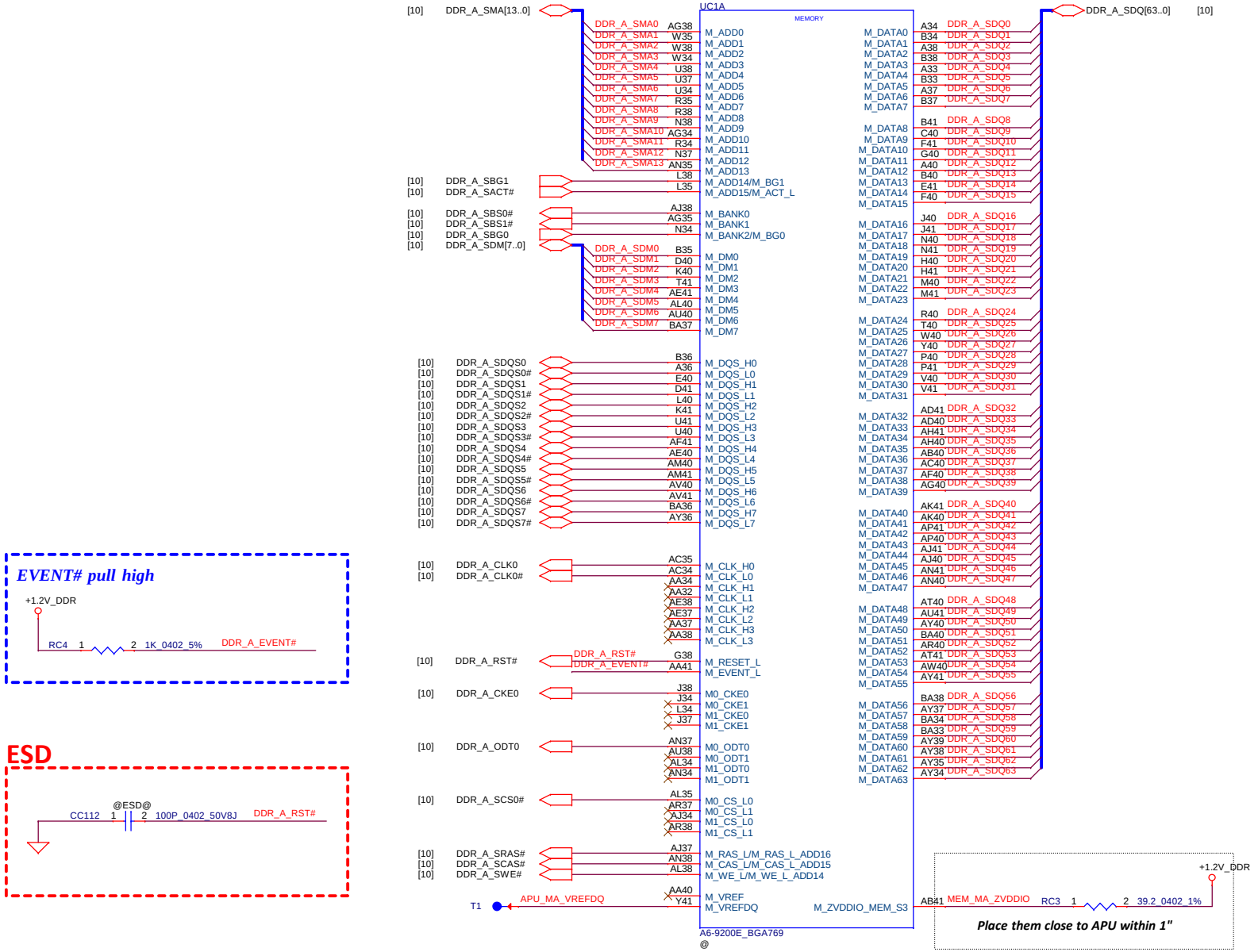

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Title: Memory

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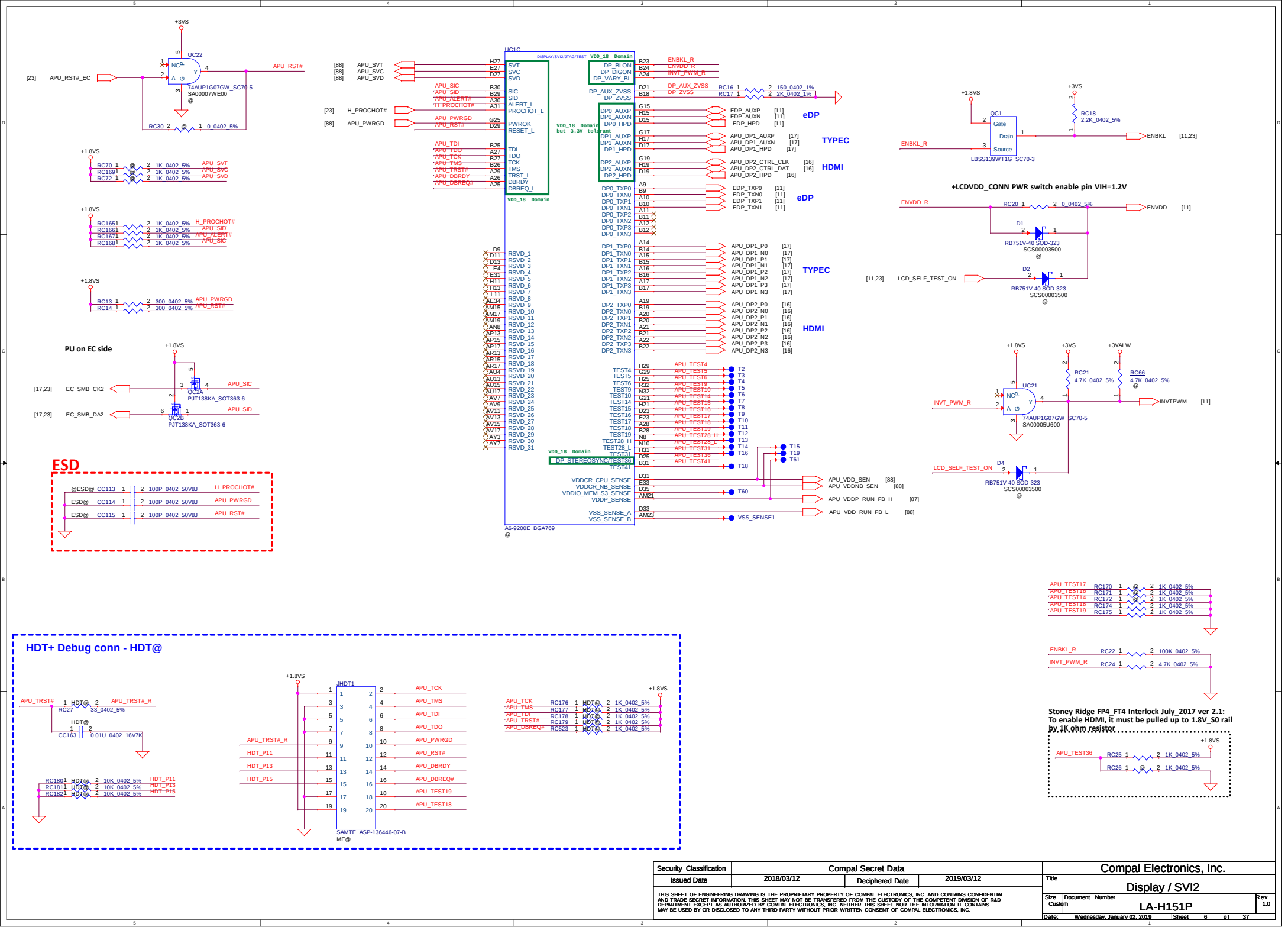

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Title: Display / SVI2

Size	Document Number	Rev
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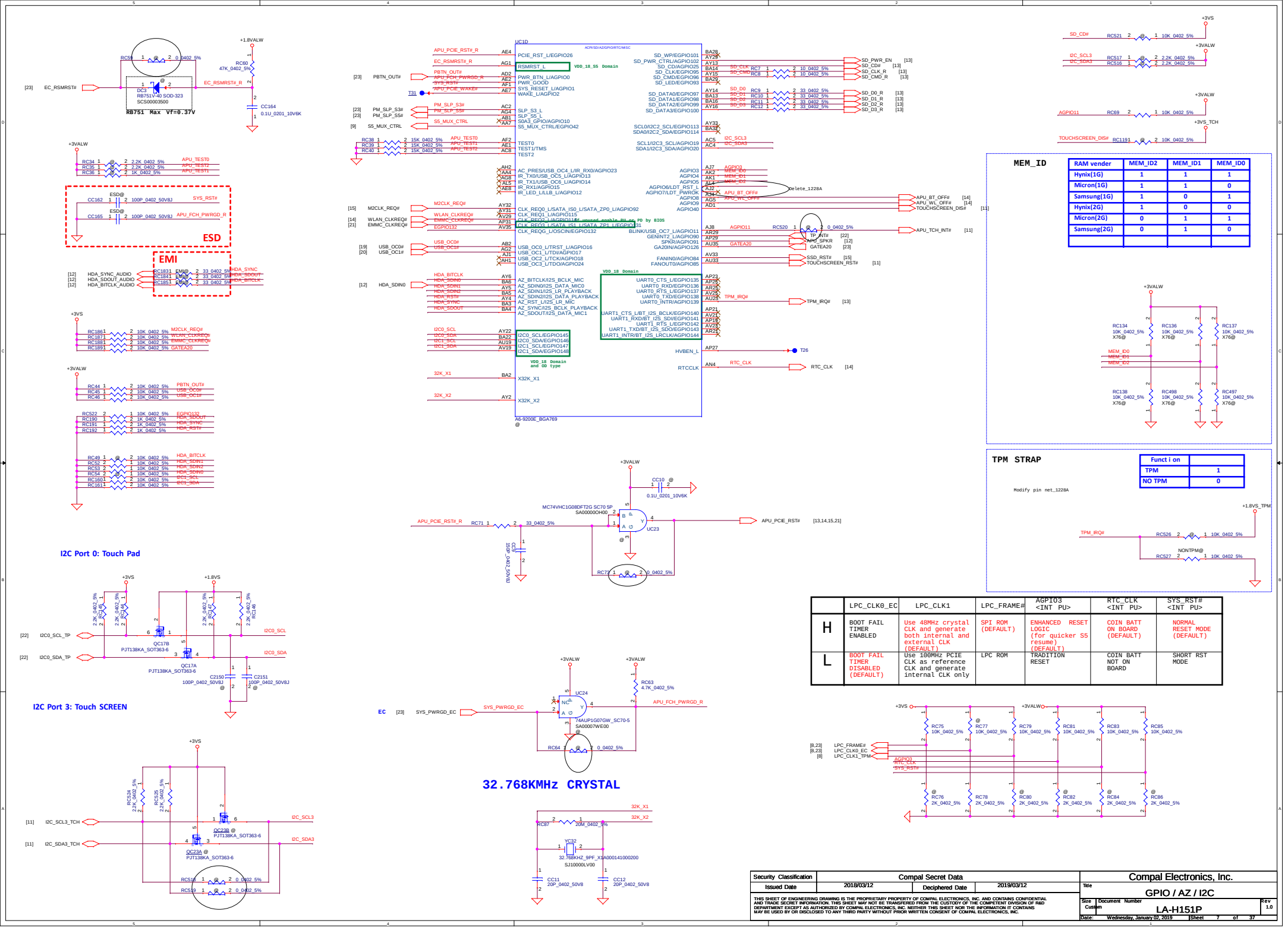
RB751 Max Vf=0.37v
I2C Port 0: Touch Pad
I2C Port 3: Touch SCREEN
32.768KMHz CRYSTAL
ESD
EMI
MEM_ID
RAM vender | MEM_ID2 | MEM_ID1 | MEM_ID0
Hynix(1G) | 1 | 1 | 1
Micron(1G) | 1 | 1 | 0
Samsung(1G) | 1 | 0 | 1
Hynix(2G) | 1 | 0 | 0
Micron(2G) | 0 | 1 | 1
Samsung(2G) | 0 | 1 | 0
TPM STRAP
Funct i on
TPM | 1
NO TPM | 0
Modify pin net_1228A
LPC_CLK0_EC | LPC_CLK1 | LPC_FRAME# | AGPIO3 <INT PU> | RTC_CLK <INT PU> | SYS_RST# <INT PU>
H | BOOT FAIL TIMER ENABLED | Use 48MHz crystal CLK and generate both internal and external CLK (DEFAULT) | SPI ROM (DEFAULT) | ENHANCED RESET LOGIC (for quicker S5 resume) (DEFAULT) | COIN BATT ON BOARD (DEFAULT) | NORMAL RESET MODE (DEFAULT)
L | BOOT FAIL TIMER DISABLED (DEFAULT) | Use 100MHz PCIE CLK as reference CLK and generate internal CLK only | LPC ROM | TRADITION RESET | COIN BATT NOT ON BOARD | SHORT RST MODE
Security Classification | Compal Secret Data
Issued Date | 2018/03/12 | Deciphered Date | 2019/03/12
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Title: GPIO / AZ / I2C
Size: Custom | Document Number: LA-H151P | Rev: 1.0
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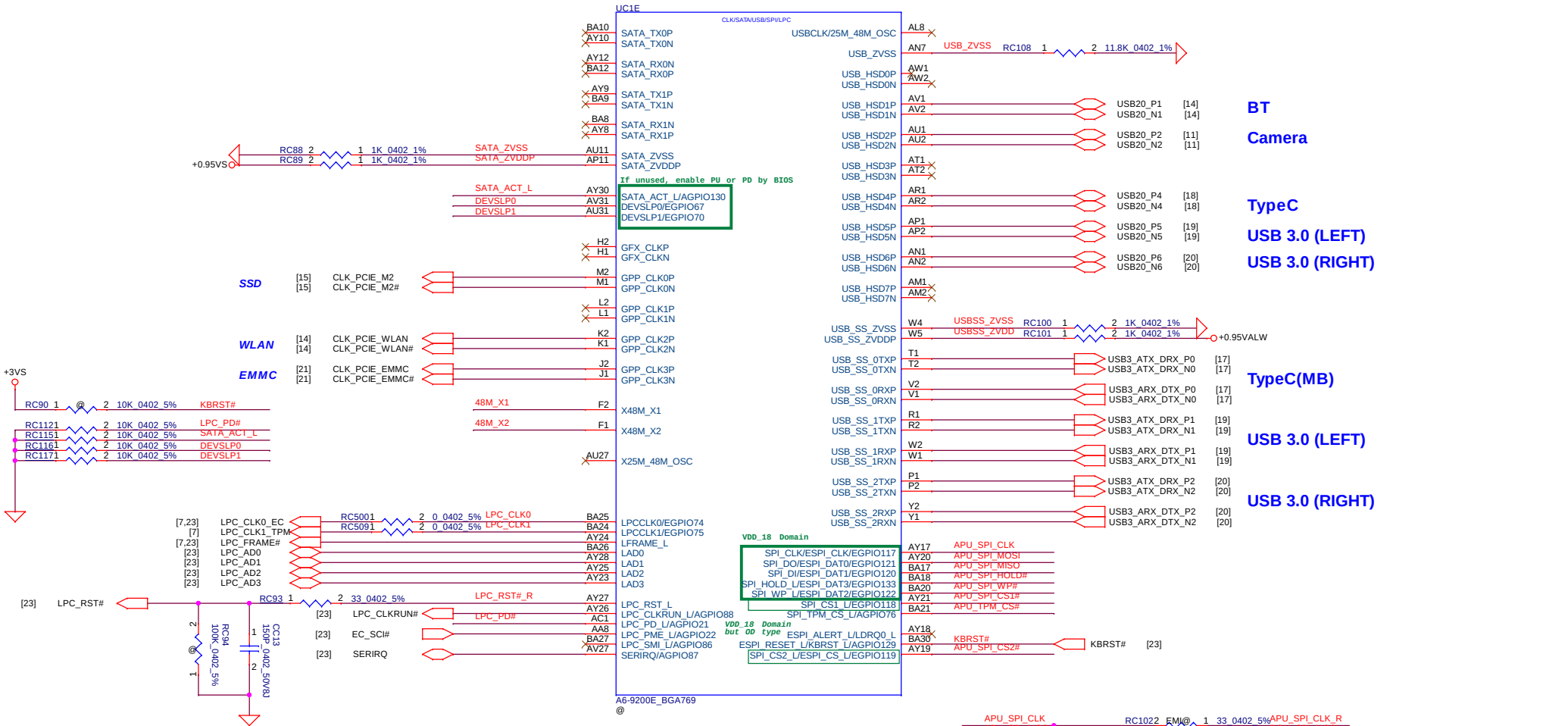

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Title: SATA / USB / LPC / SPI

Size	Document Number	Rev
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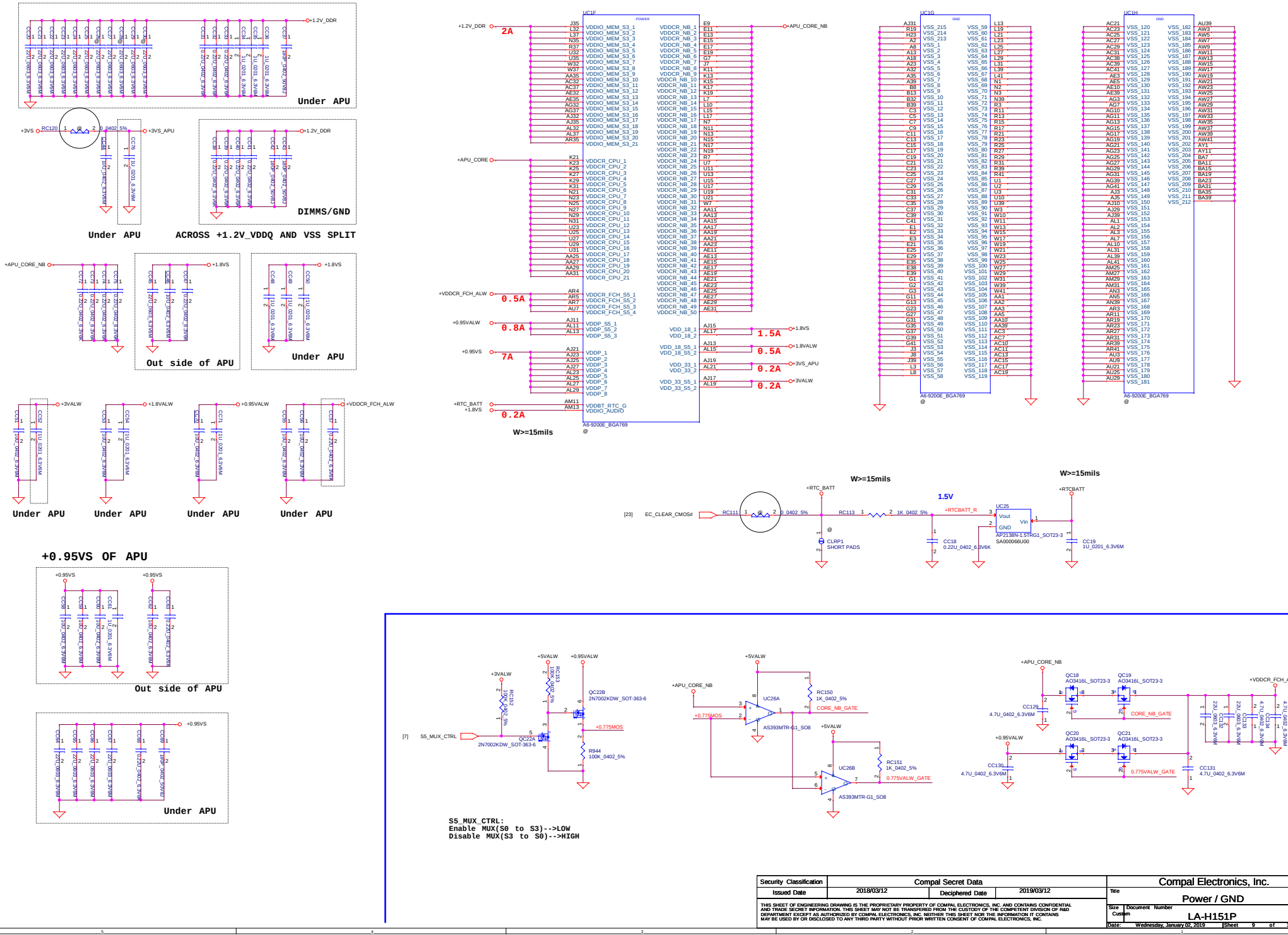
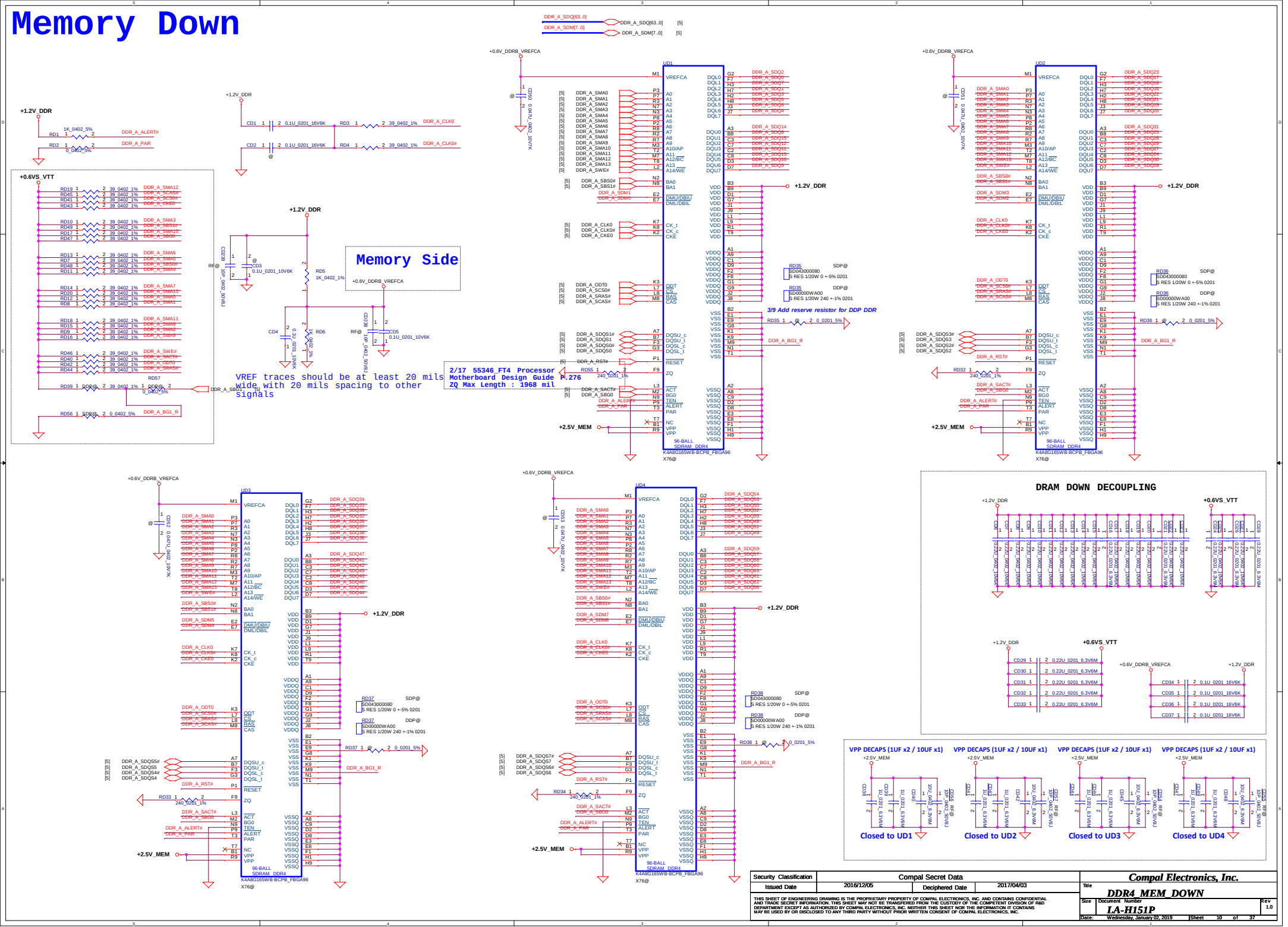

Under APU
ACROSS +1.2V_VDDQ AND VSS SPLIT
DIMMS/GND
Out side of APU
+0.95VS OF APU
UC1F
UC1G
UC1H
2A
0.5A
0.8A
7A
0.2A
1.5A
W>=15mils
1.5V
S5_MUX_CTRL:
Enable MUX(S0 to S3)-->LOW
Disable MUX(S3 to S0)-->HIGH
Compal Secret Data
Compal Electronics, Inc.
Power / GND
LA-H151P
2018/03/12
2019/03/12
Wednesday, January 02, 2019

Memory Down



Security Classification	Compal Secret Data		
Issued Date	2016/12/05	Deciphered Date	2017/04/03

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Title: **DDR4_MEM_DOWN**

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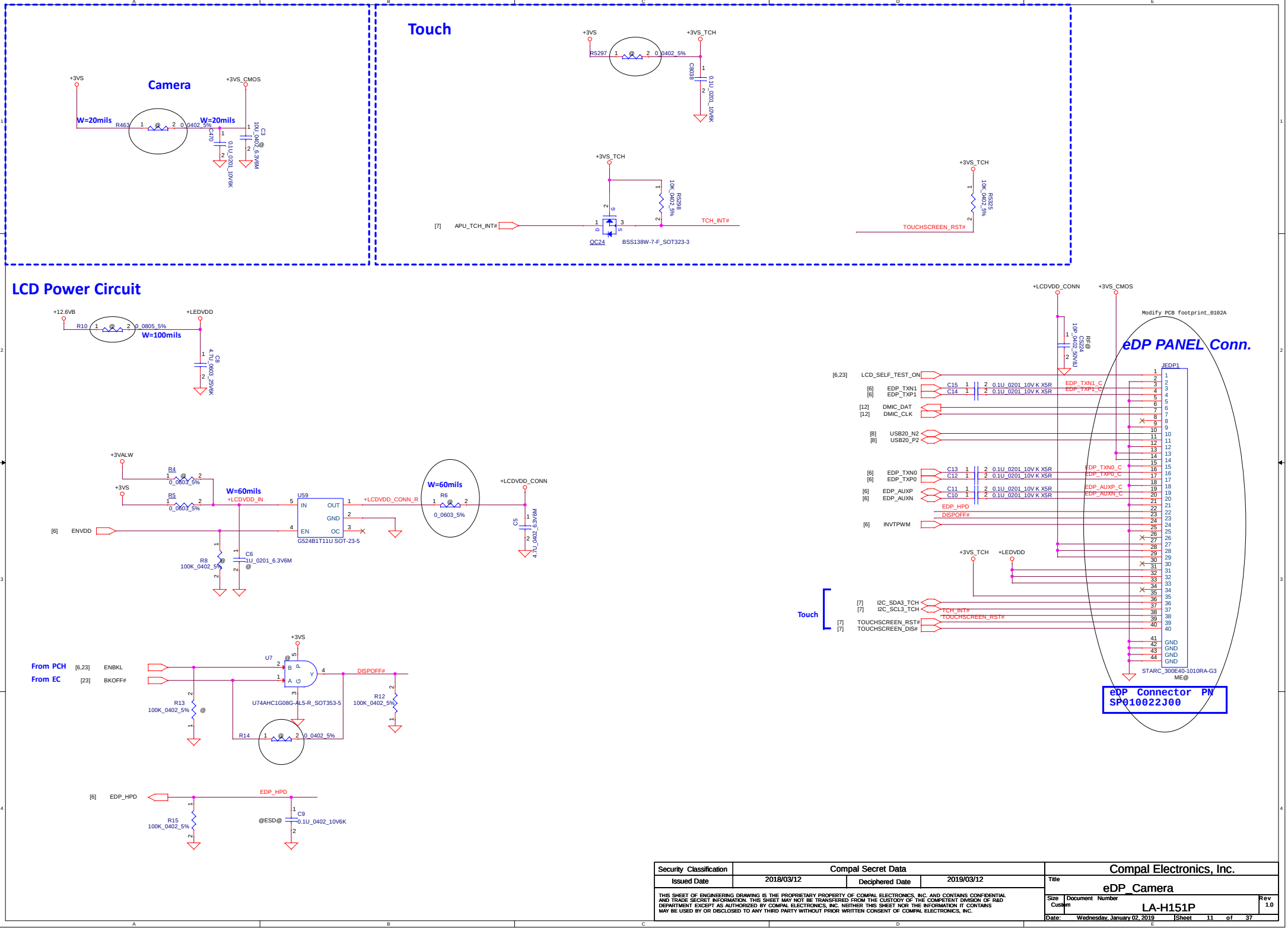

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Compal Electronics, Inc.			
Title	eDP_Camera		
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ALC3287

U60

ALC3287-CG_MQFN48_6X6

I2C_DATA
I2C_CLK
SYNC
BCLK
SDATA-OUT
DC_DET/EPAD
SDATA-IN
NC
NC
NC
NC
NC
SPDIF-OUT/GPIO2/DMIC-DATA34/DMIC-CLK-IN
GPIO0/DMIC-DATA12
GPIO1/DMIC-CLK
PDB
JD1
JD2
VREF
LDO1-CAP
MIC2-CAP
MIC2-VREFO-R
MIC2-VREFO-L
CPVEE
CBN
CBP
LDO2-CAP
LDO3-CAP

PCBEEP
MIC2-L/RING2
MIC2-R/SLEEVE
LINE2-L
LINE2-R
SPK-OUT-L+
SPK-OUT-L-
SPK-OUT-R-
SPK-OUT-R+
HPOUT-L
HPOUT-R

5VSTB
AVDD1
CPVDD/AVDD2
DVDD
DVDD-IO
PVDD1
PVDD2
Thermal_Pad
AVSS1
AVSS2

HDA_SYNC_AUDIO
HDA_BITCLK_AUDIO
HDA_SDOUT_AUDIO
HDA_SDIN0
HDA_SDIN0_AUDIO
DMIC_DAT
DMIC_CLK
EC_MUTE#
PLUG_IN

PC_BEEP
EXT_MIC_RING2
EXT_MIC_SLEEVE
SPK_L+
SPK_L-
SPK_R-
SPK_R+
HP_OUTL
HP_OUTR

AGND
GND

R3338 Change to 0ohm form Vendor agree

+5AVDD_CODEC
+1.8AVDD_CODEC
+1.8DVDD
+1.8DVDDIO
+5VS
+5VSPVDD

For vendor suggest +5AVDD_CODEC use VS power

close to Pin40

+1.8VS

PC Beep

place close audio codec

BEEP#
APU_SPKR
BEEP_N
PC_BEEP

Speaker

wide 40MIL

Speaker Connector PN SP020015V00

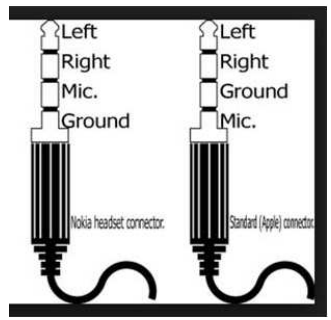
EMI
ESD

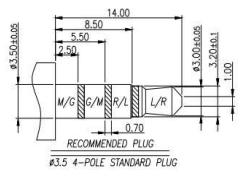
SPK_R+
SPK_R-
SPK_L+
SPK_L-
SPK_R+_CONN
SPK_R-_CONN
SPK_L+_CONN
SPK_L-_CONN

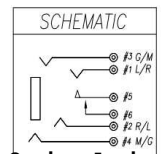
JSPK1 ME@
ACES_50277-0040N-001
GND1
GND2

D54 @ESD@ L03ESDL5V0CC3-2_SOT23-3 SCA00002900
D55 @ESD@ L03ESDL5V0CC3-2_SOT23-3 SCA00002900

Mono speaker will output form Left channel by Vendor relpy







Combo Jack (Normal Open)

wide 60MIL

W=40mils
W=40mils

MIC2-VREFO-L
EXT_MIC_RING2
HP_OUTL
HP_OUTR
EXT_MIC_SLEEVE
MIC2-VREFO-R
PLUG_IN

HPOUT_L
HPOUT_R
HPOUT_L1
HPOUT_R1

JHP1
SINGA_2SJ3080-001111F
DC23000B300
ME@

Audio Connector PN DC23000B300

EMI
ESD

D53 @ESD@ L03ESDL5V0CC3-2_SOT23-3
D52 ESD@ L03ESDL5V0CC3-2_SOT23-3

Bidirectional ESD protection of two lines
PartNumber SCA00000T00

Security Classification	Compal Secret Data		
Issued Date	2014/09/01	Deciphered Date	2015/09/01

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Title: HD Audio Codec_ALC3287

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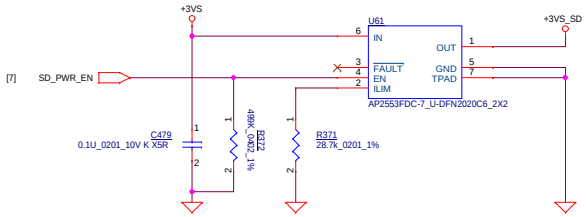
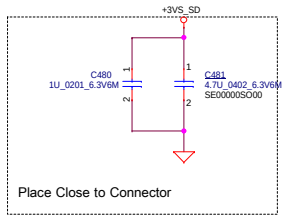
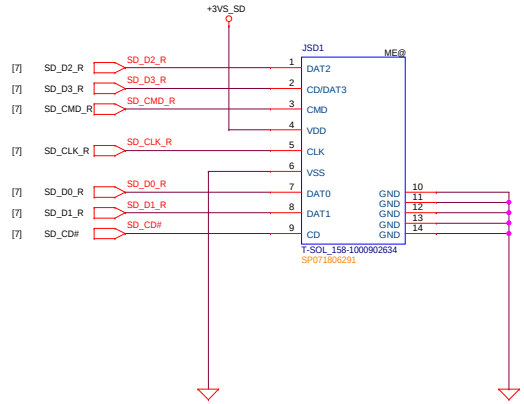
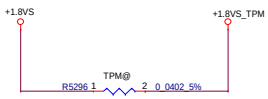
CARD READER

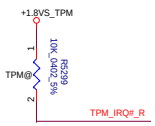


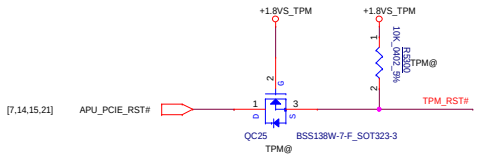


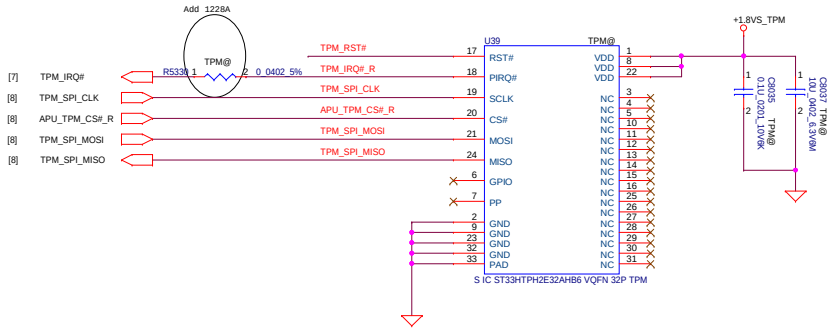


TPM









Security Classification	Compal Secret Data		
Issued Date	2018/03/12	Deciphered Date	2019/03/12

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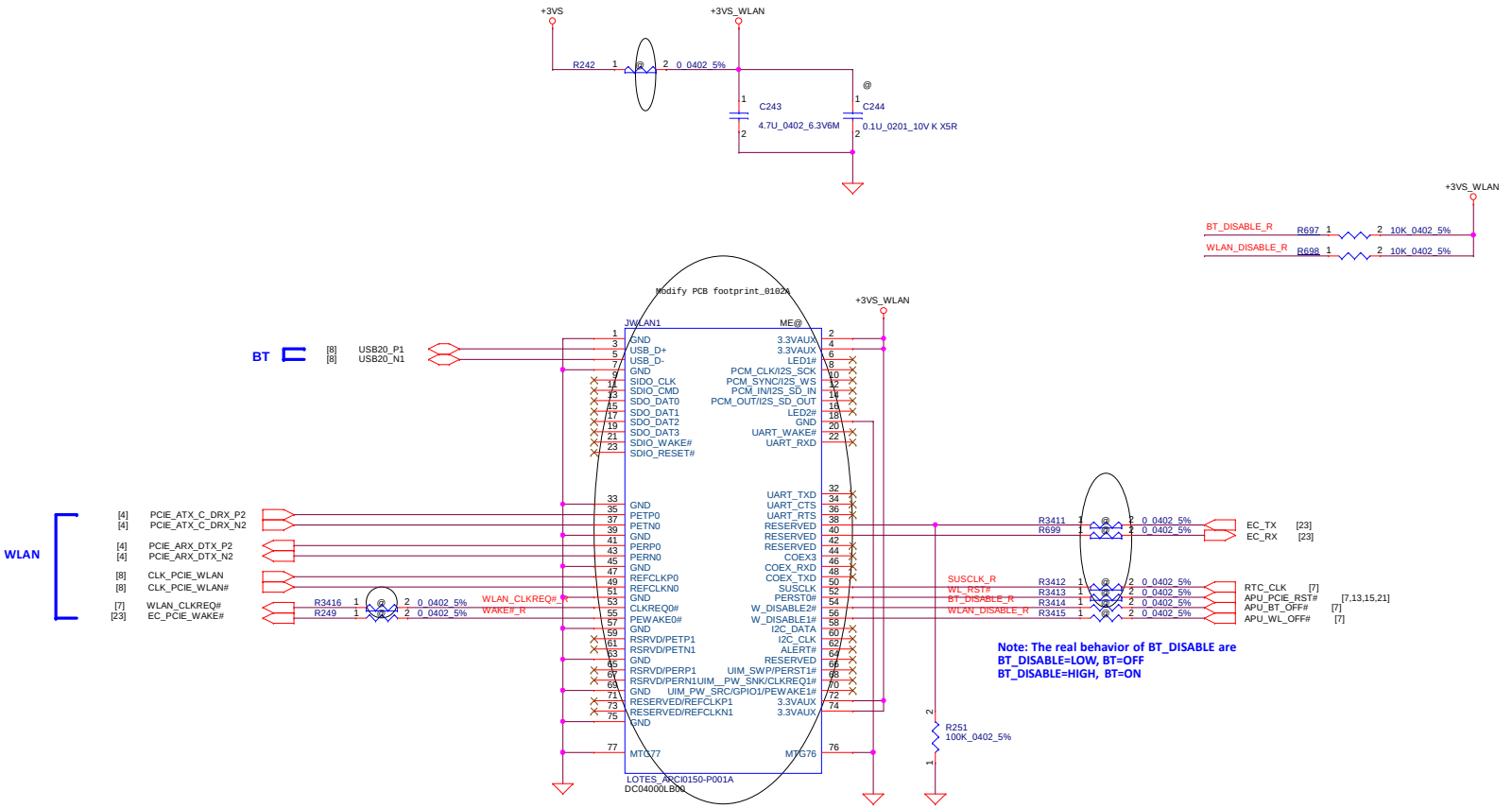
Compal Electronics, Inc.

Title: Card Reader_TPM

Size	Document Number	Rev
C	LA-H151P	1.0

Date: Wednesday, January 02, 2019 Sheet 13 of 37

NGFF - WLAN / BT (E- KEY)



Security Classification	Compal Secret Data		
Issued Date	2018/03/12	Deciphered Date	2019/03/12

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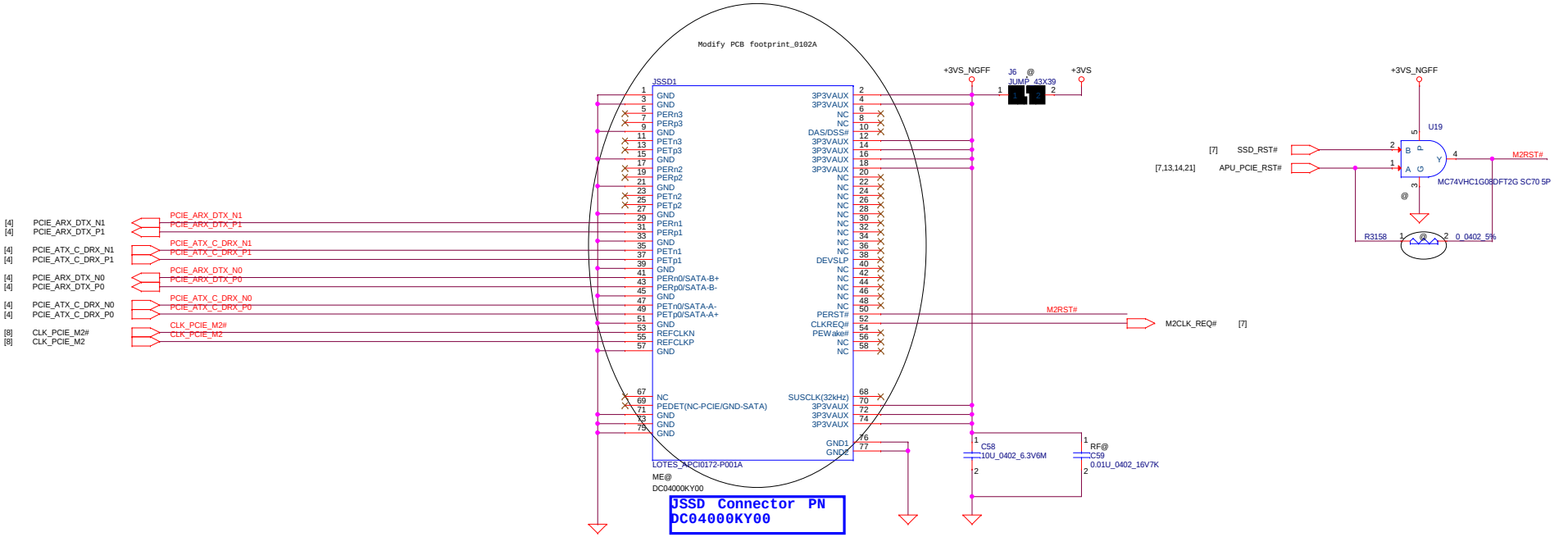
Compal Electronics, Inc.			
Title	NGFF WLAN / BT		
Size	Document Number		Rev
	LA-H151P		1.0
Date: Wednesday, January 02, 2019	Sheet 14 of 37		

M.2 mSATA Conn



Security Classification	Compal Secret Data		
Issued Date	2016/12/05	Deciphered Date	2017/04/03

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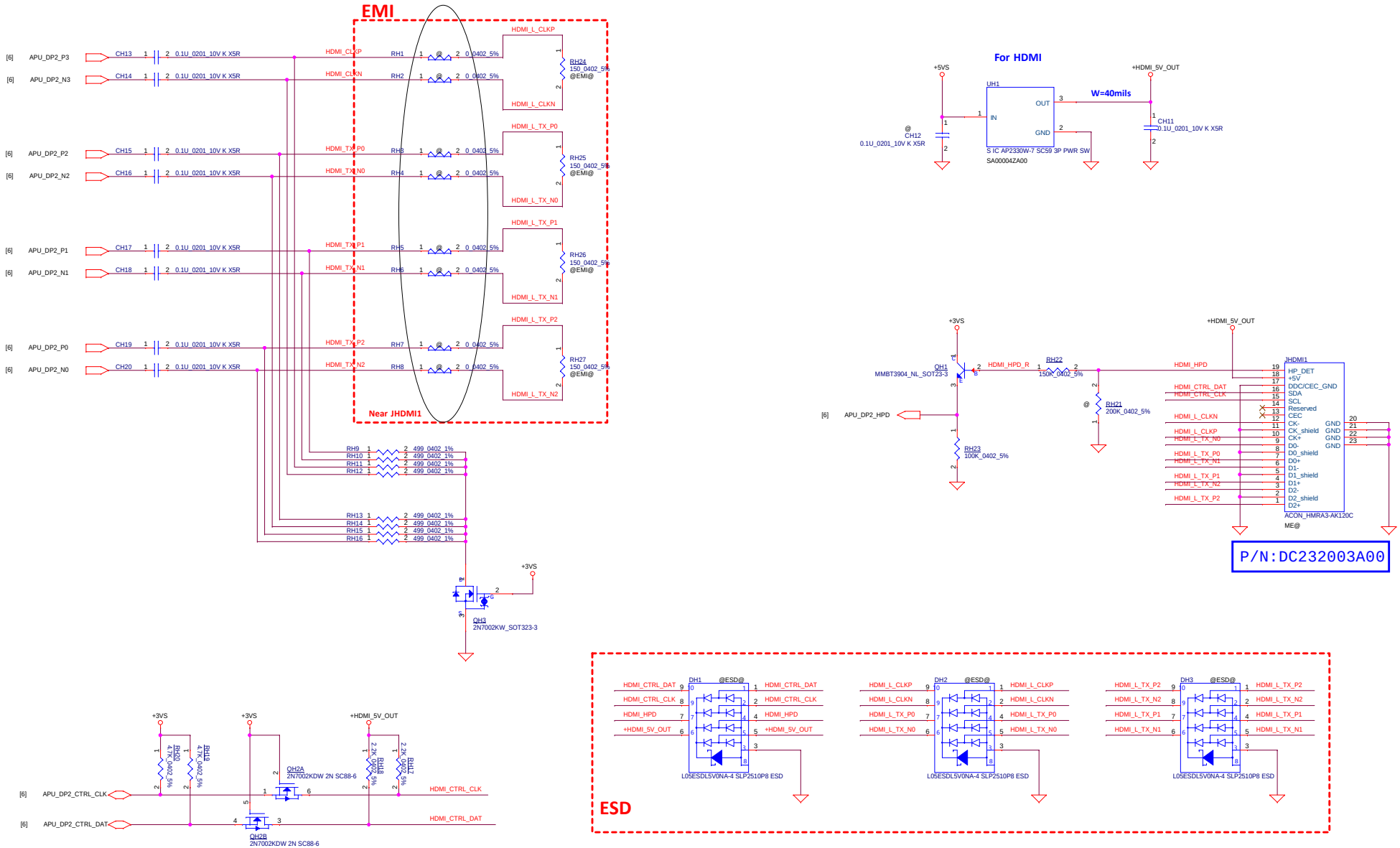
Compal Electronics, Inc.

Title: **M.2 SSD/HDD**

Size	Document Number	Rev
Custom	LA-H151P	0.1

Date: Wednesday, January 02, 2019 | Sheet 15 of 37



Security Classification	Compal Secret Data		
Issued Date	2015/03/06	Deciphered Date	2016/12/31

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Compal Electronics, Inc.

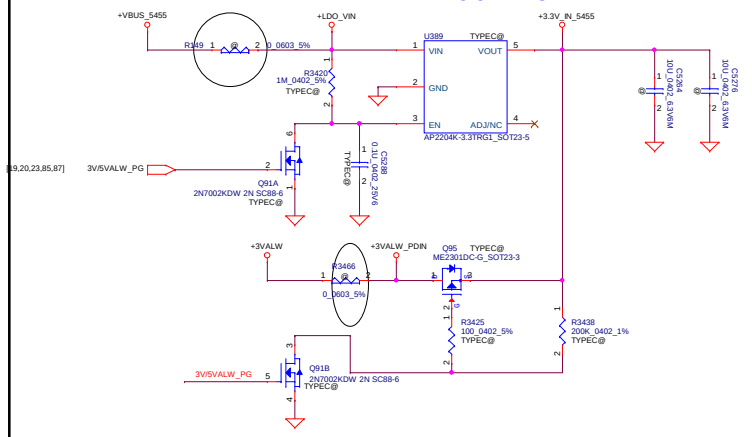
Title: **HDMI Conn**

Size	Document Number	Rev
C	LA-H151P	0.1

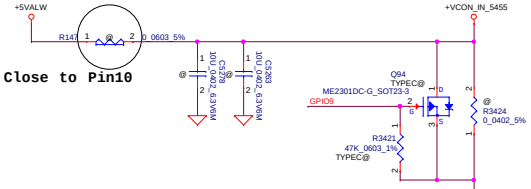
Date: Wednesday, January 02, 2019 Sheet 16 of 37

dead battery

PD VIN 3.3V LDO



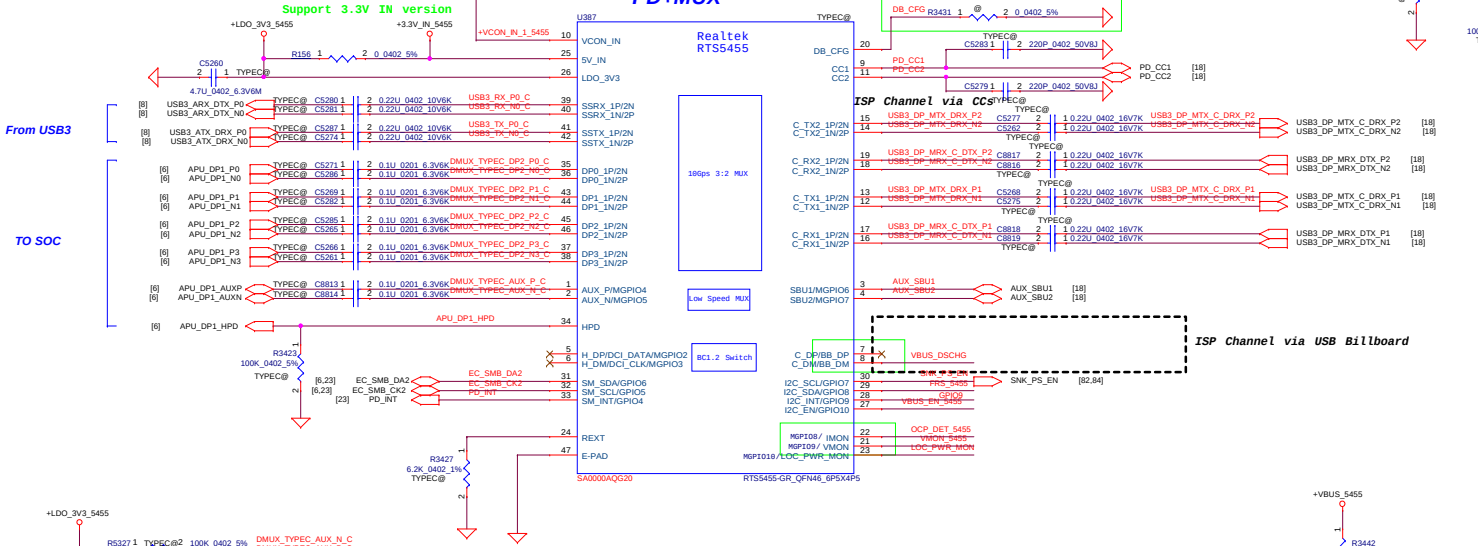
Close to Pin10

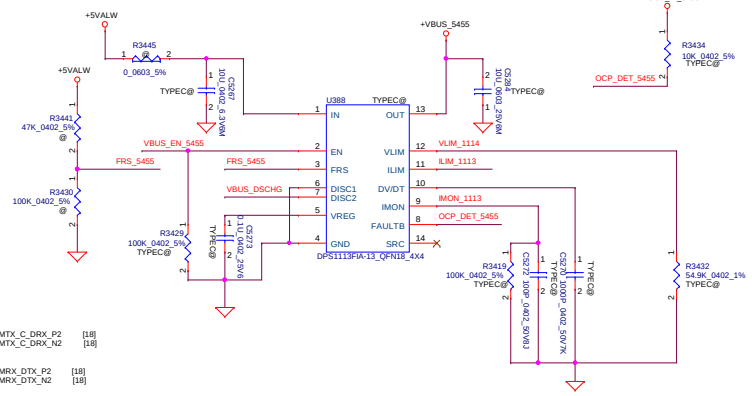


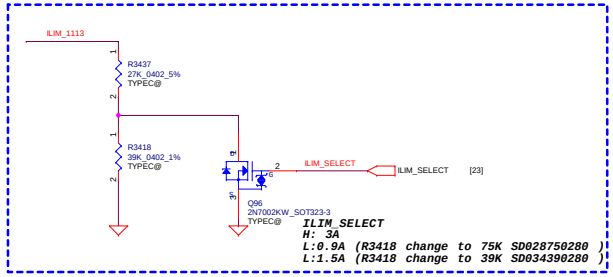
SYMBOL
PD+MUX

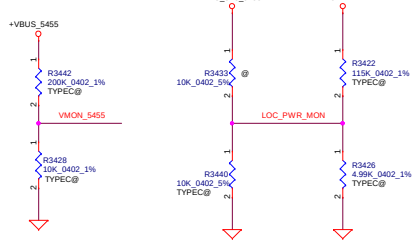
Dead battery function Cfig. pin.
Tie to GND to disable dead battery ' Rd' .
Floating to enable dead battery ' Rd'

Support 3.3V IN version



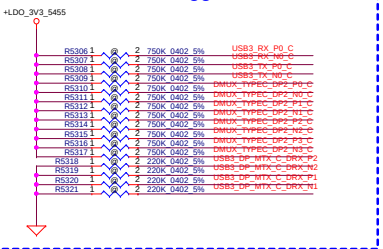




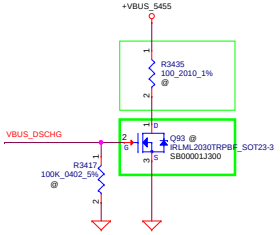


0314_Add
Connect 'LOC_PWR' net to local power for F/W to decide if C port can become provider via PR_SWAP. Leave floating if no local power exists in the system or in the application that 545x can only be powered on by local power.

Add for vendor suggestion



VBUS Discharge



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Issued Date	2017/08/02	Deciphered Date	2018/08/02

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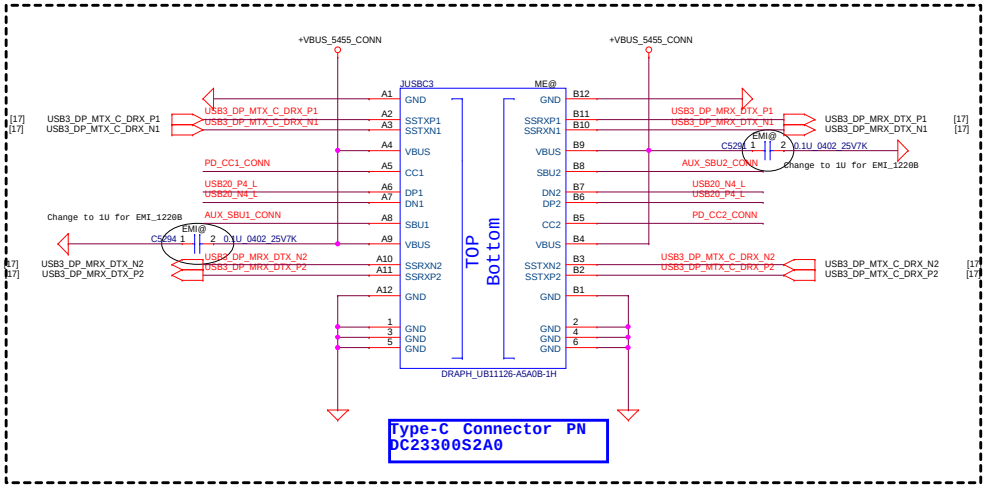
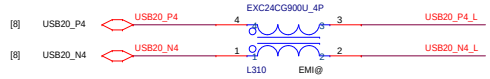
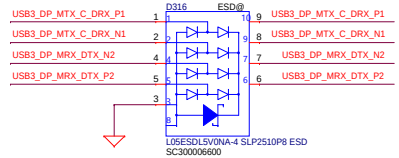
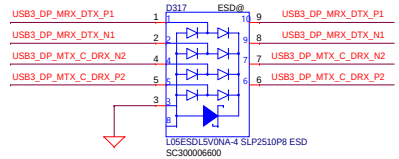
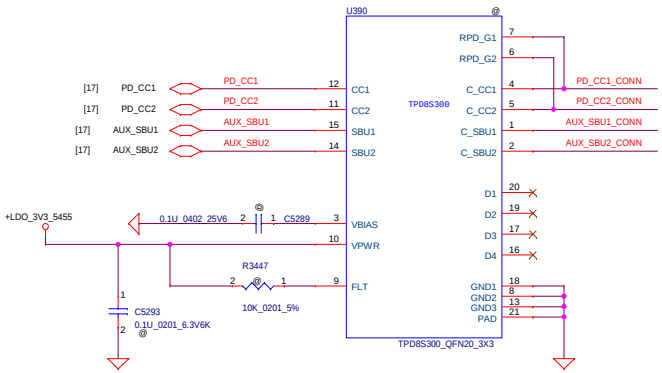
Compal Electronics, Inc.			
Title: Type-C RTS5455			
Size: Custom	Document Number: LA-H151P		Rev: 0.3
Date: Wednesday, January 02, 2019	Sheet 17 of 37		

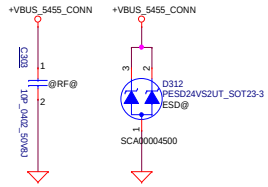




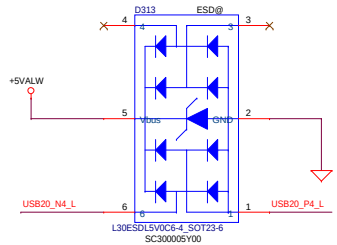


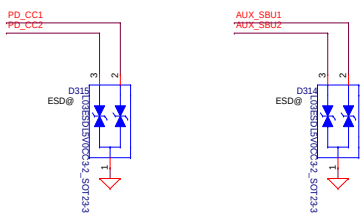






ESD for USBC1 Lines and Control lines





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Issued Date		Deciphered Date	

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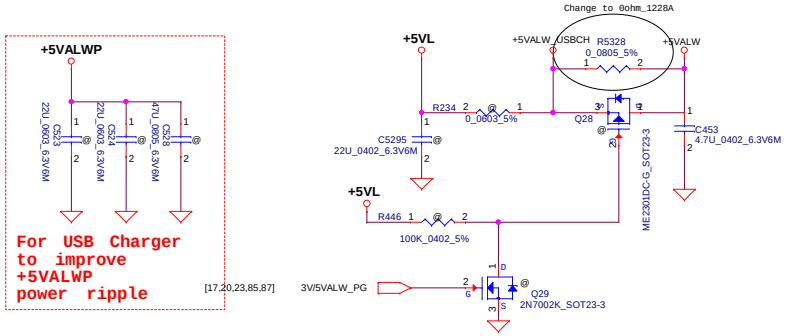
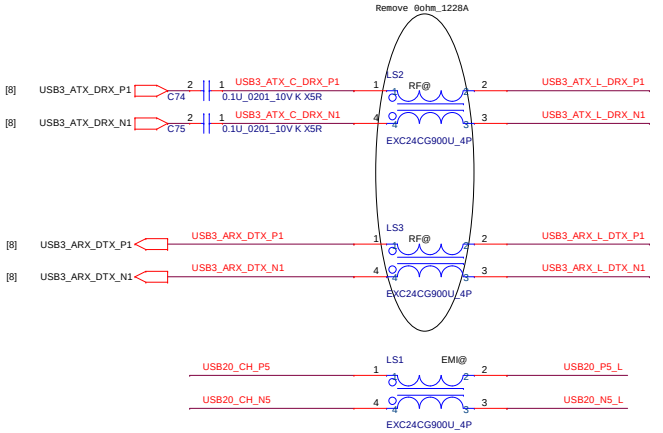
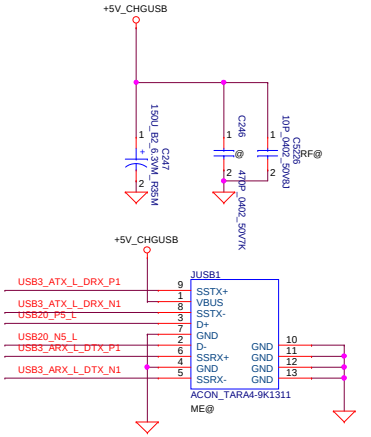
Compal Electronics, Inc.			
Title: Type-C_RTS5455_CONN			
Size: C	Document Number: LA-H151P		Rev: 0.3
Date: Wednesday, January 02, 2019		Sheet 18 of 37	

USB 3.0 (LEFT)

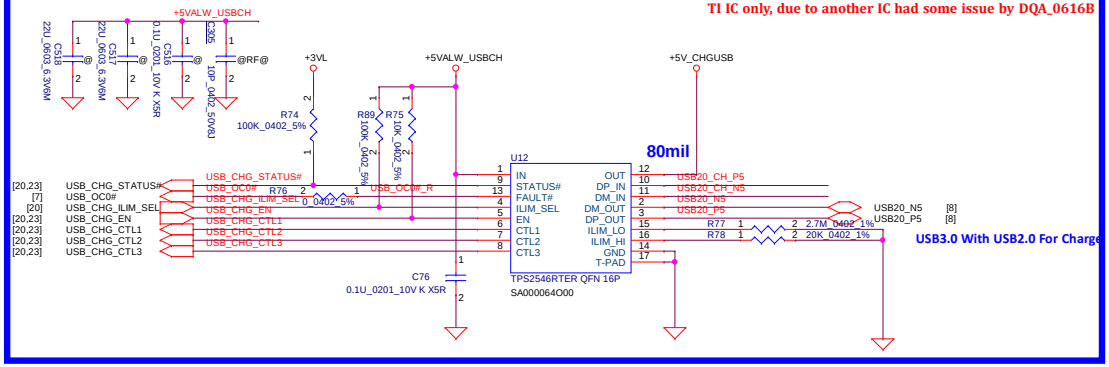






USB3.0 Connector PN DC233007010

AOU



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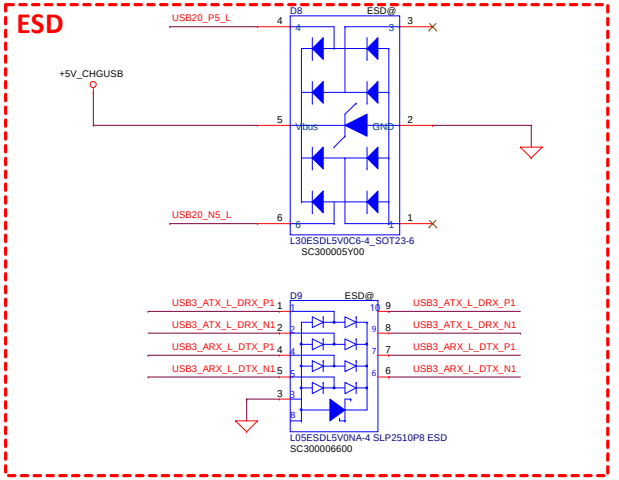

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Issued Date	2018/03/12	Deciphered Date	2019/03/12

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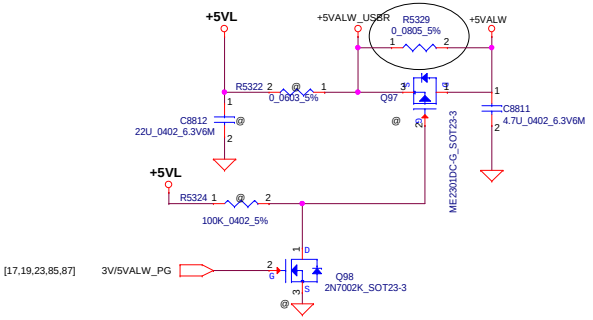
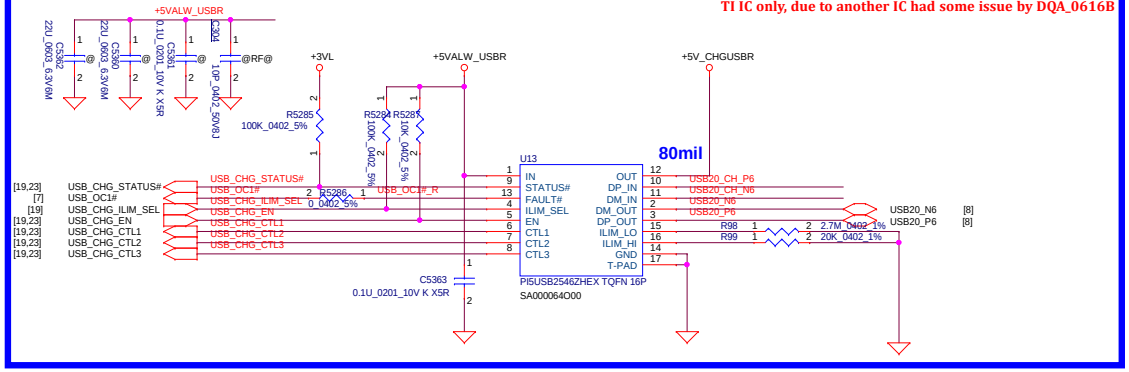
Title			
USB3.0			
Size: Custom	Document Number: LA-H151P		Rev: 1.0
Date: Wednesday, January 02, 2019	Sheet 19 of 37		

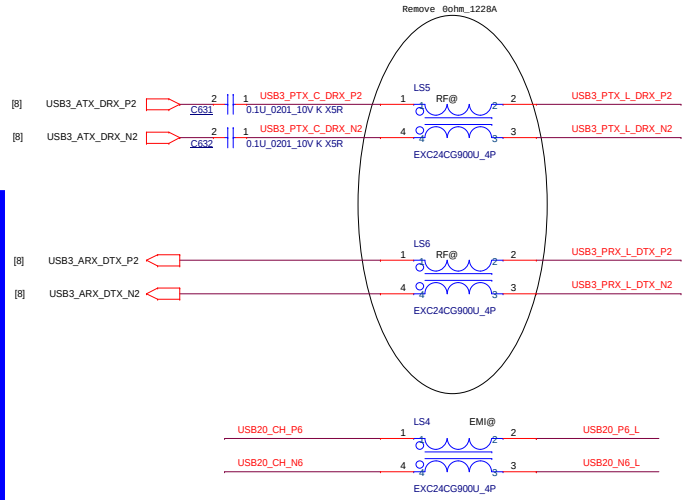
USB3.0(Right)

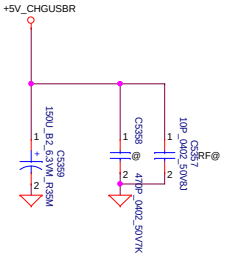
Change to 0ohm_1228A

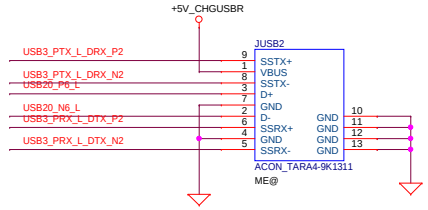


TI IC only, due to another IC had some issue by DQA_0616B









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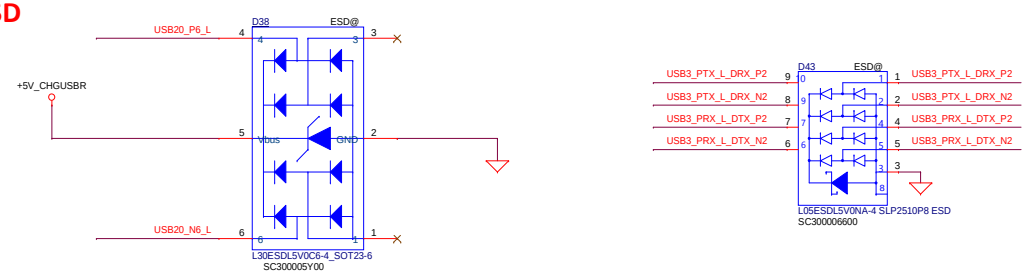

Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2016/12/31

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Compal Electronics, Inc.

Title: **USB3_Right**

Size	Document Number	Rev
Custom	LA-H151P	0.1

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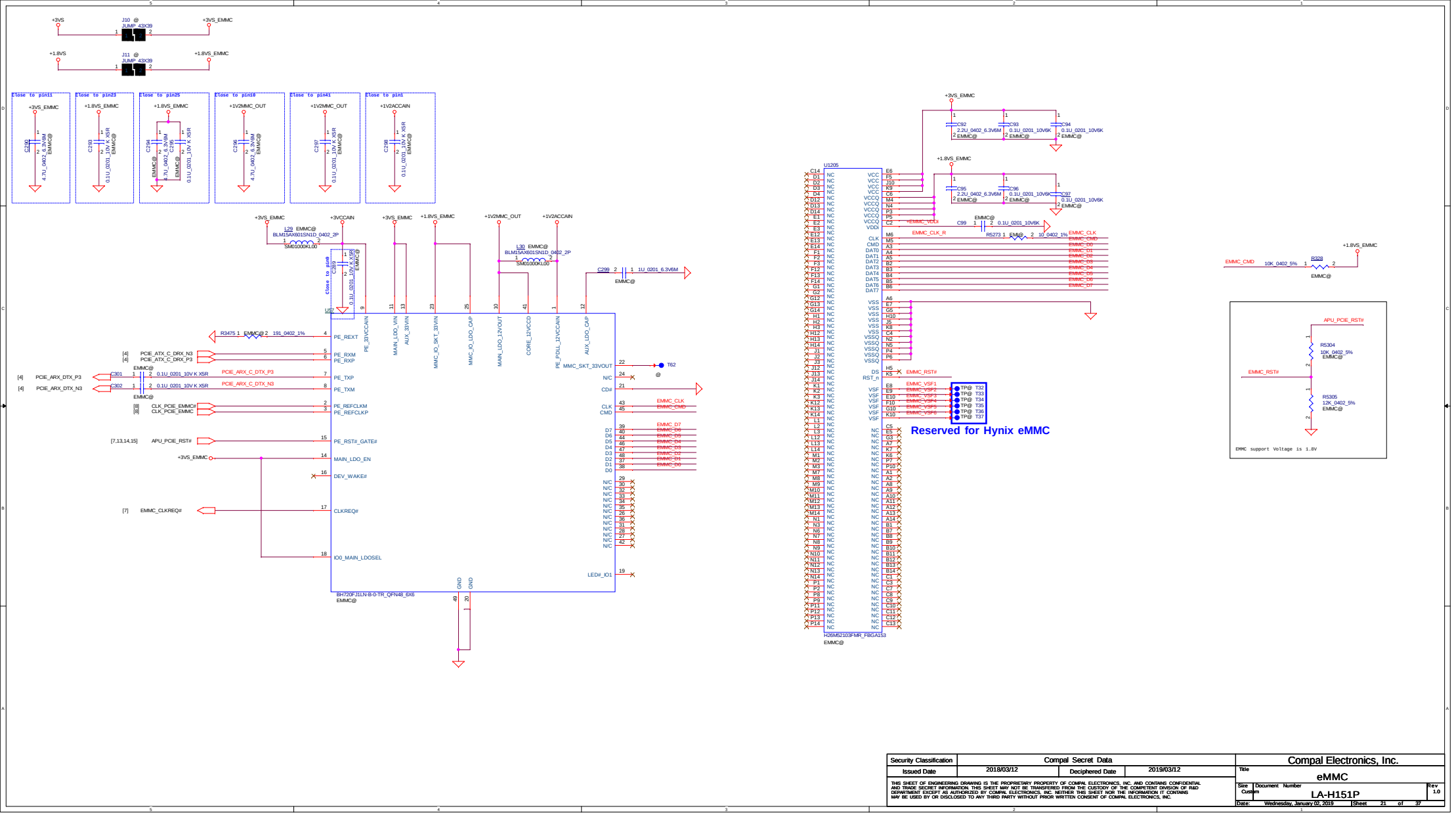

Security Classification	Compal Secret Data		
Issued Date	2018/03/12	Deciphered Date	2019/03/12

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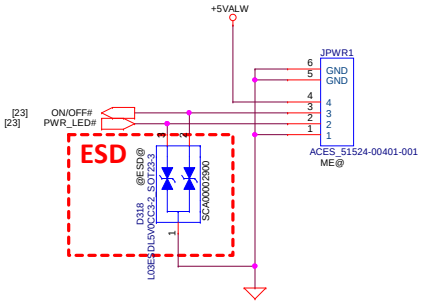
Compal Electronics, Inc.

Title: eMMC

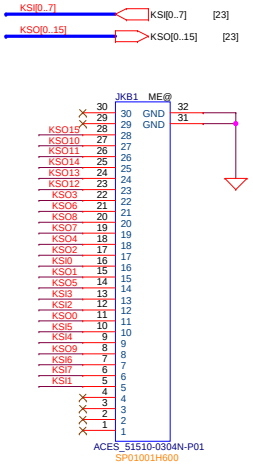
Size	Document Number	Rev
Custom	LA-H151P	1.0

Date: Wednesday, January 02, 2019 Sheet 21 of 37

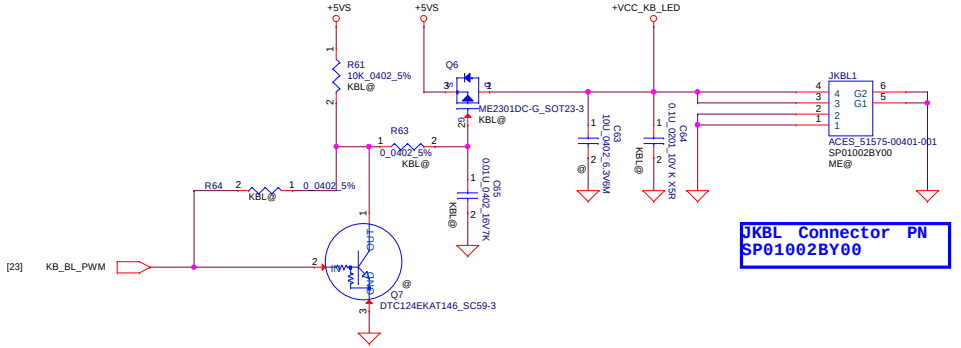
PWR BTN Board



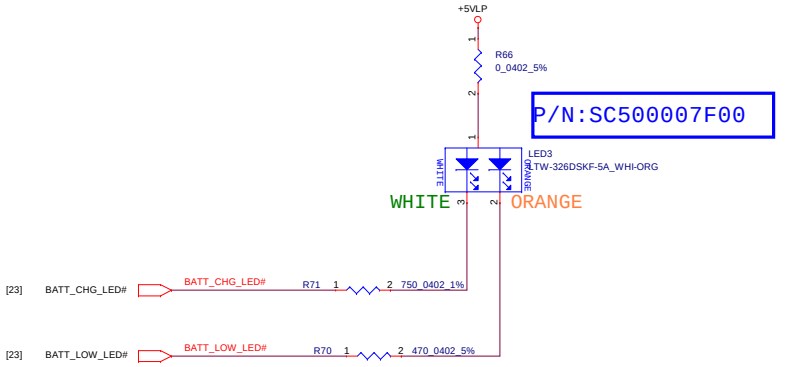
Keyboard



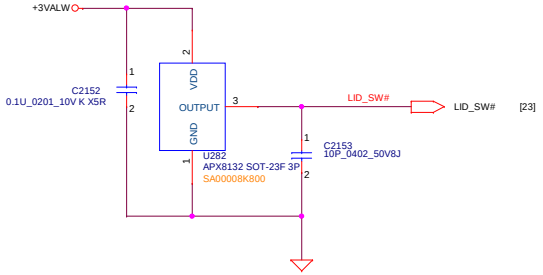
Keyboard Backlight



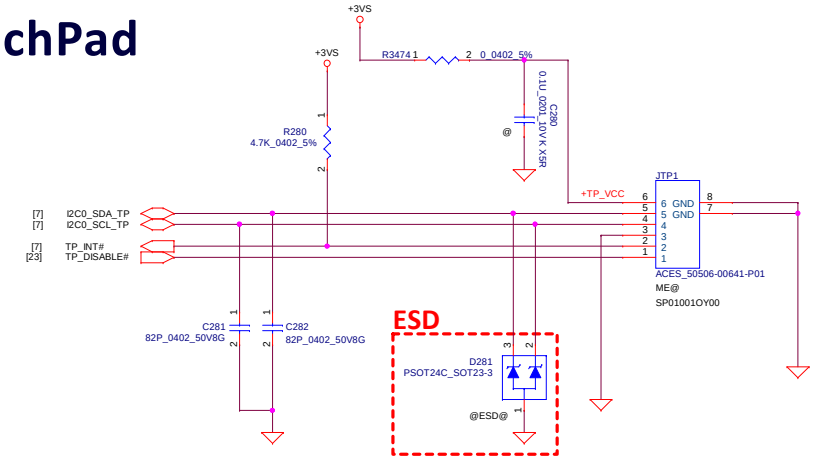
Charge LED



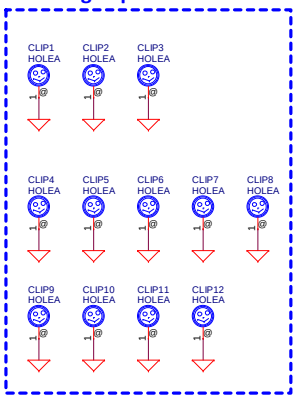
Hall Sensor



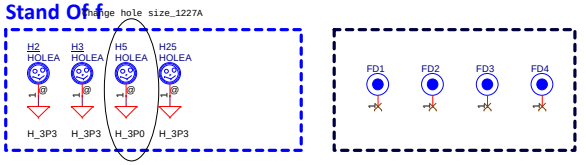
TouchPad



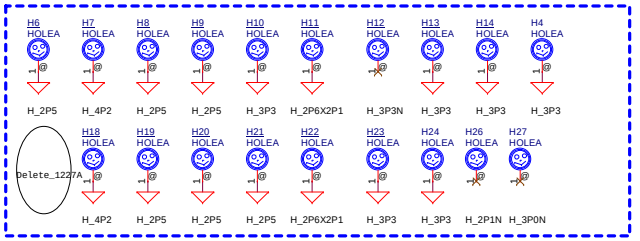
Shielding Clip



Stand Off



Screw Hole



Security Classification	Compal Secret Data		
Issued Date	2018/03/12	Deciphered Date	2019/03/12

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Compal Electronics, Inc.	
Title	KBD/Hall Sensor/TP
Size: Custom	Document Number: LA-H151P
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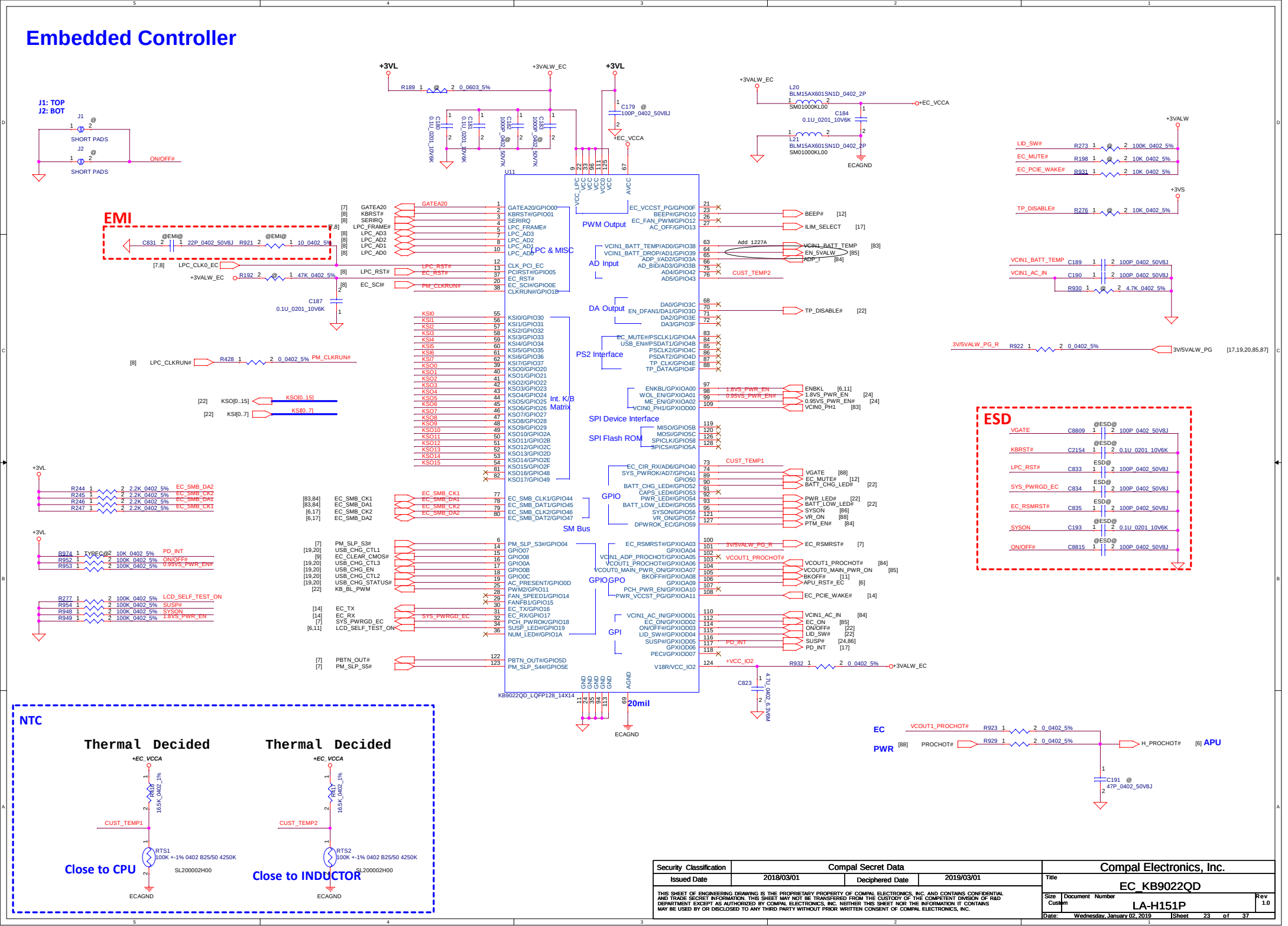
Date: Wednesday, January 02, 2019	Sheet 22 of 37

Embedded Controller



Security Classification	Compal Secret Data		
Issued Date	2018/03/01	Deciphered Date	2019/03/01

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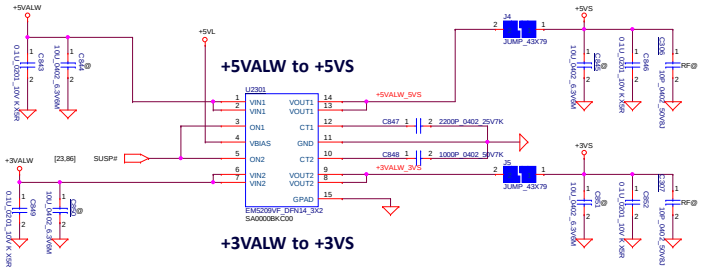
Compal Electronics, Inc.

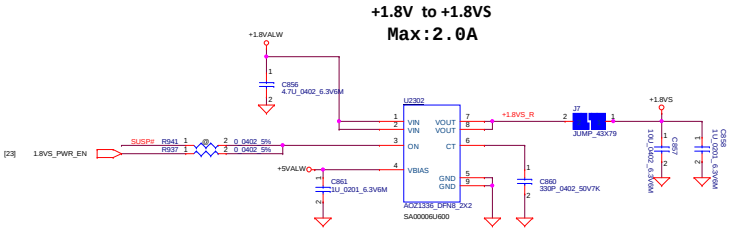
Title: EC_KB9022QD

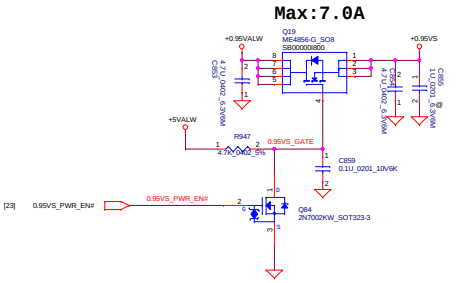
Size	Document Number	Rev
Custom	LA-H151P	1.0

Date: Wednesday, January 02, 2019 | Sheet 23 of 37

DC to DC







Security Classification	Compal Secret Data		
Issued Date	2018/03/12	Deciphered Date	2019/03/12

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Compal Electronics, Inc.

Title: DC to DC /Discgarge /MISC

Size: Custom | Document Number: LA-H151P | Rev: 1.0

Date: Wednesday, January 02, 2019 | Sheet 24 of 37

Security Classification	Compal Secret Data		
Issued Date	2018/03/12	Deciphered Date	2019/03/12

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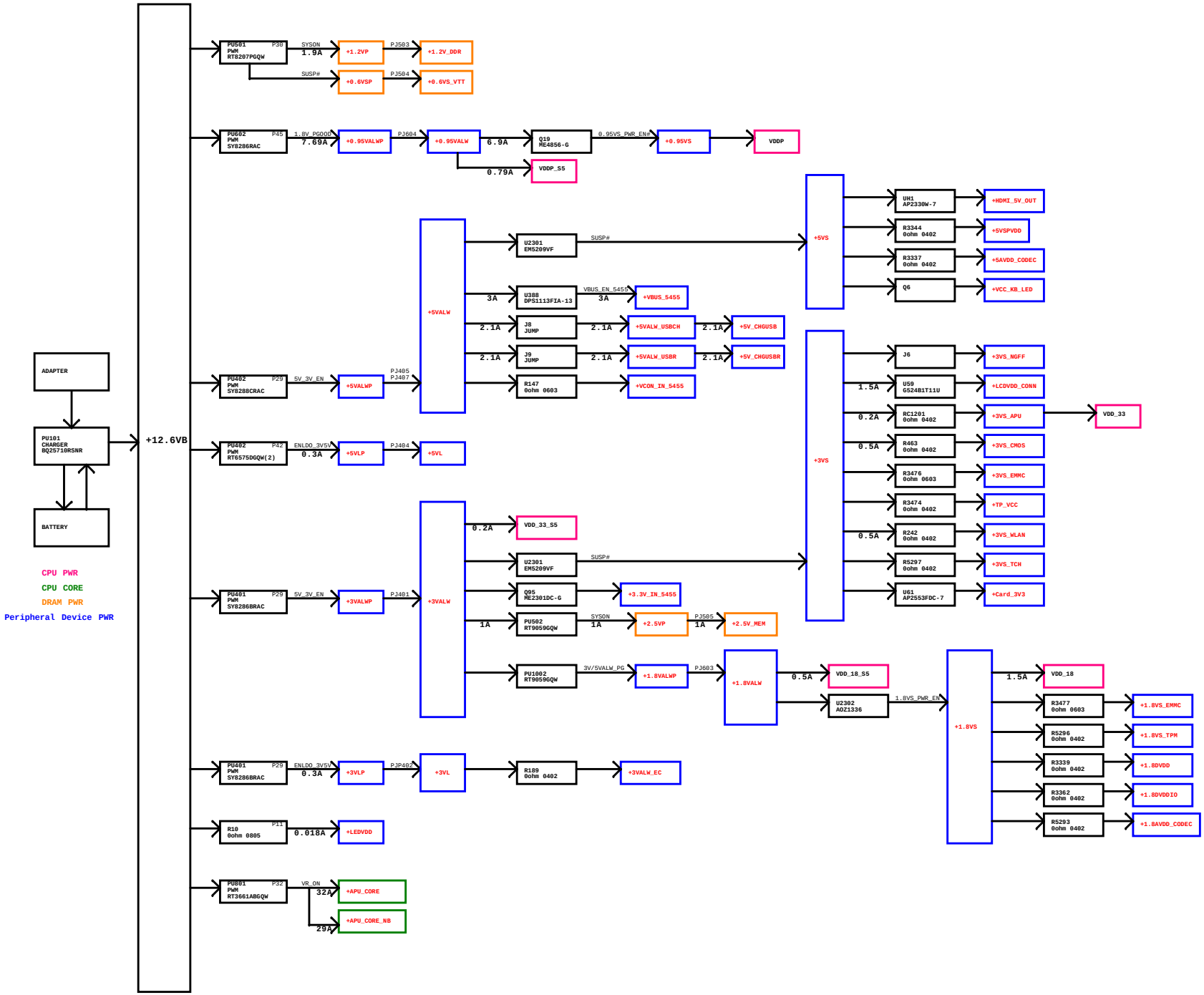
Compal Electronics, Inc.

Title: Reserve

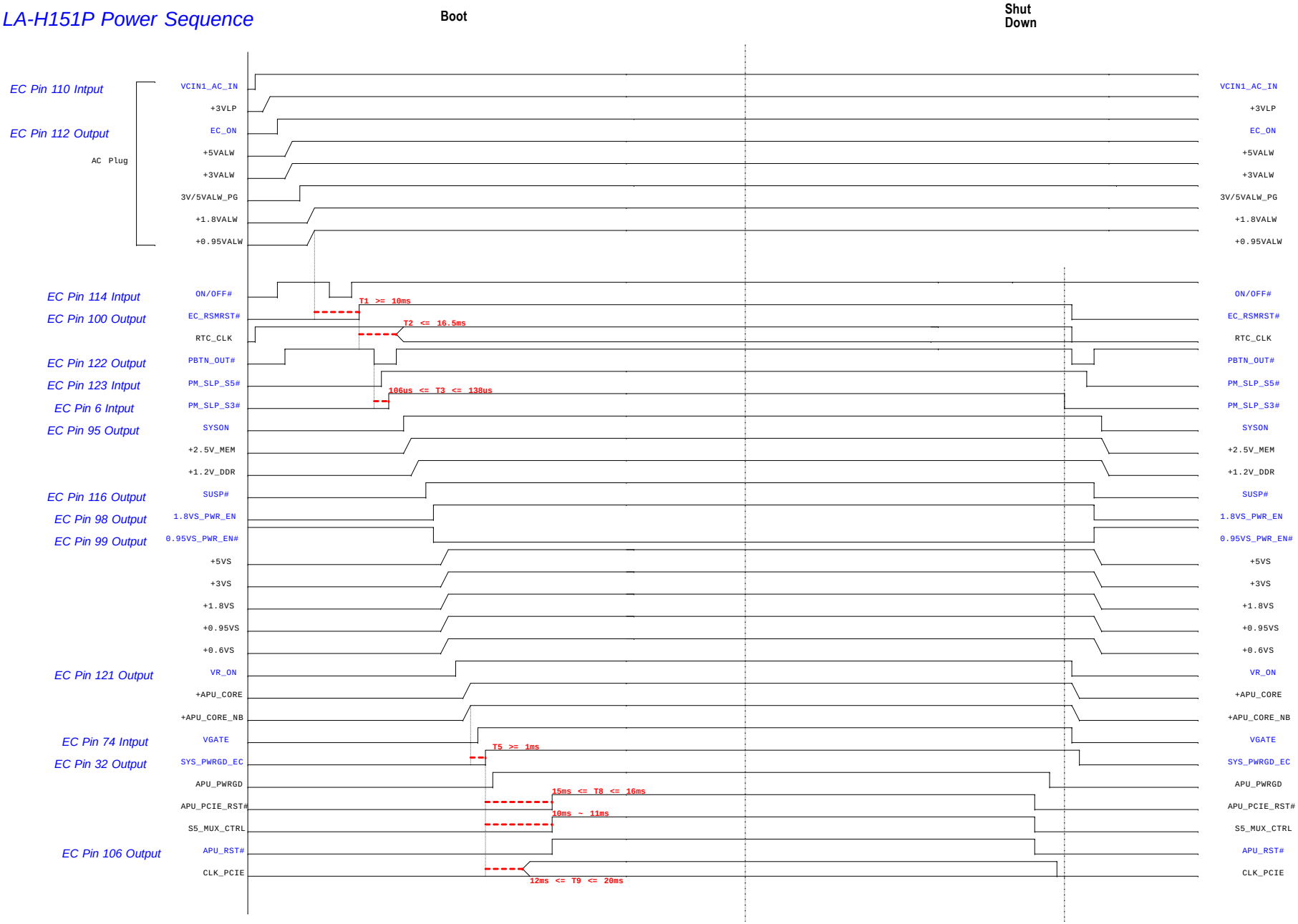
Size	Document Number	Rev
Custom	LA-H151P	1.0

Date: Wednesday, January 02, 2019 Sheet 25 of 37



Title	Power MAP	
Size C	Document Number LA-H151P	Rev 1.0
Date: Wednesday, January 02, 2019	Sheet 26 of 37	

LA-H151P Power Sequence



Title: Power Sequence			
Size: C	Document Number: LA-H151P		Rev: 1.0
Date: Wednesday, January 02, 2019	Sheet 27 of 37		

HW SIT PIR List

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	18/10/03	7	Delete RC129, RC130	For double reserve
2	18/10/03	7	Add RC526	Reserve WL_OFF pull up
3	18/10/08	22	Modify Screw hole size	For DfX request
4	18/10/17	22	Change R71 value to 750 ohm	For LED brightness
5	18/10/26	23	Change R244, R245 pull update power source	For Type C function
6	18/11/02	17	Add C8813/8814, R5326/5327	For Type C AUX communication
7	18/11/08	7, 14	Delete RC41, RC526, add R698, R697	For prevent leakage from BT_OFF & WL_OFF
8	18/11/08	17	Add C8816~8819	Prevent some dongle issue
9	18/11/12	7	Change RC9~12 value to 33 ohm	Base on EMI test result
10				
11				
12				
13				
14				
15				
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Security Classification	Compal Secret Data		
Issued Date	2018/03/12	Deciphered Date	2017/04/03

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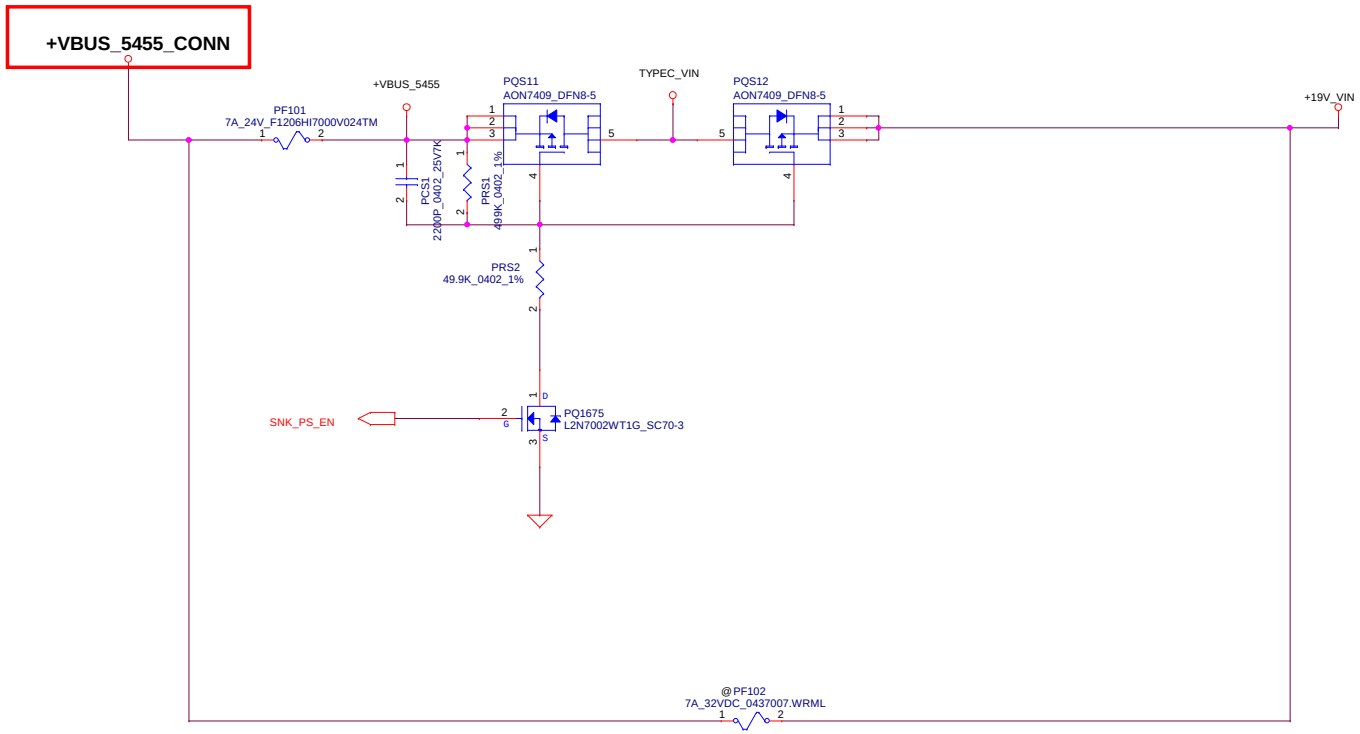
Compal Electronics, Inc.

Title			
HW PIR			
Size: C	Document Number: LA-H151P		Rev: 0.2
Date: Wednesday, January 02, 2019	Sheet 28 of 37		



Security Classification	Compal Secret Data		
Issued Date	2017/03/09	Deciphered Date	2018/06/30

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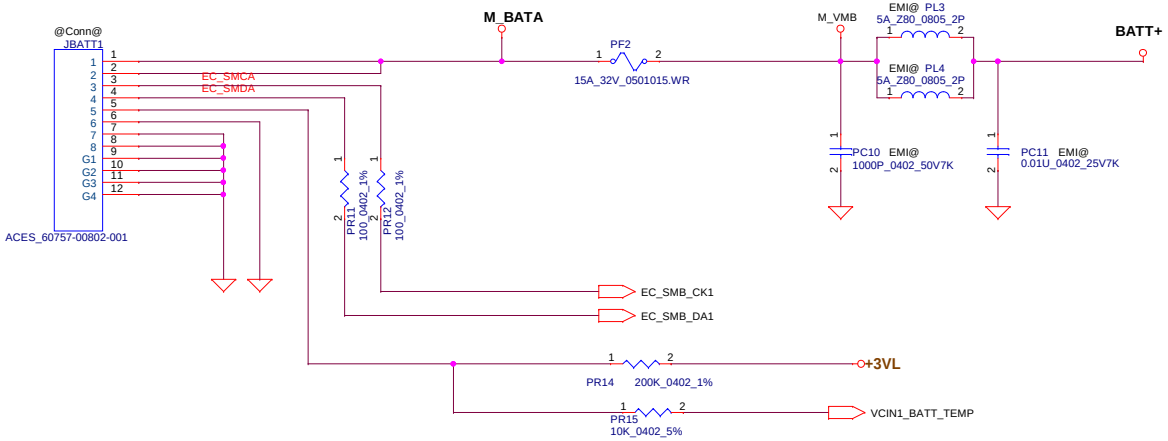
Compal Electronics, Inc.

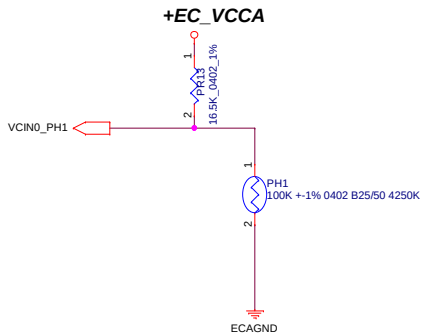
Title: **PWR-DCIN / Vin Detector**

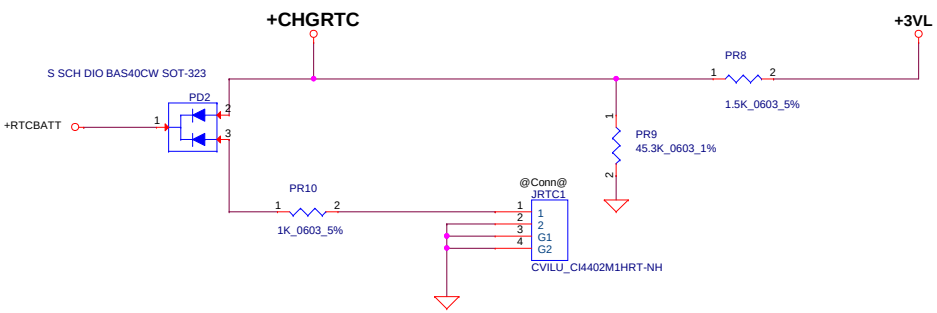
Size: Custom | Document Number: **LA-H151P** | Rev: 1.0

Date: Wednesday, January 02, 2019 | Sheet 82 of 37



PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C





Security Classification	Compal Secret Data		
Issued Date	2017/03/09	Deciphered Date	2018/06/30

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Compal Electronics, Inc.

Title: **PWR-BATTERY CONN/OTP**

Size	Document Number	Rev
Custom	LA-H151P	1.0

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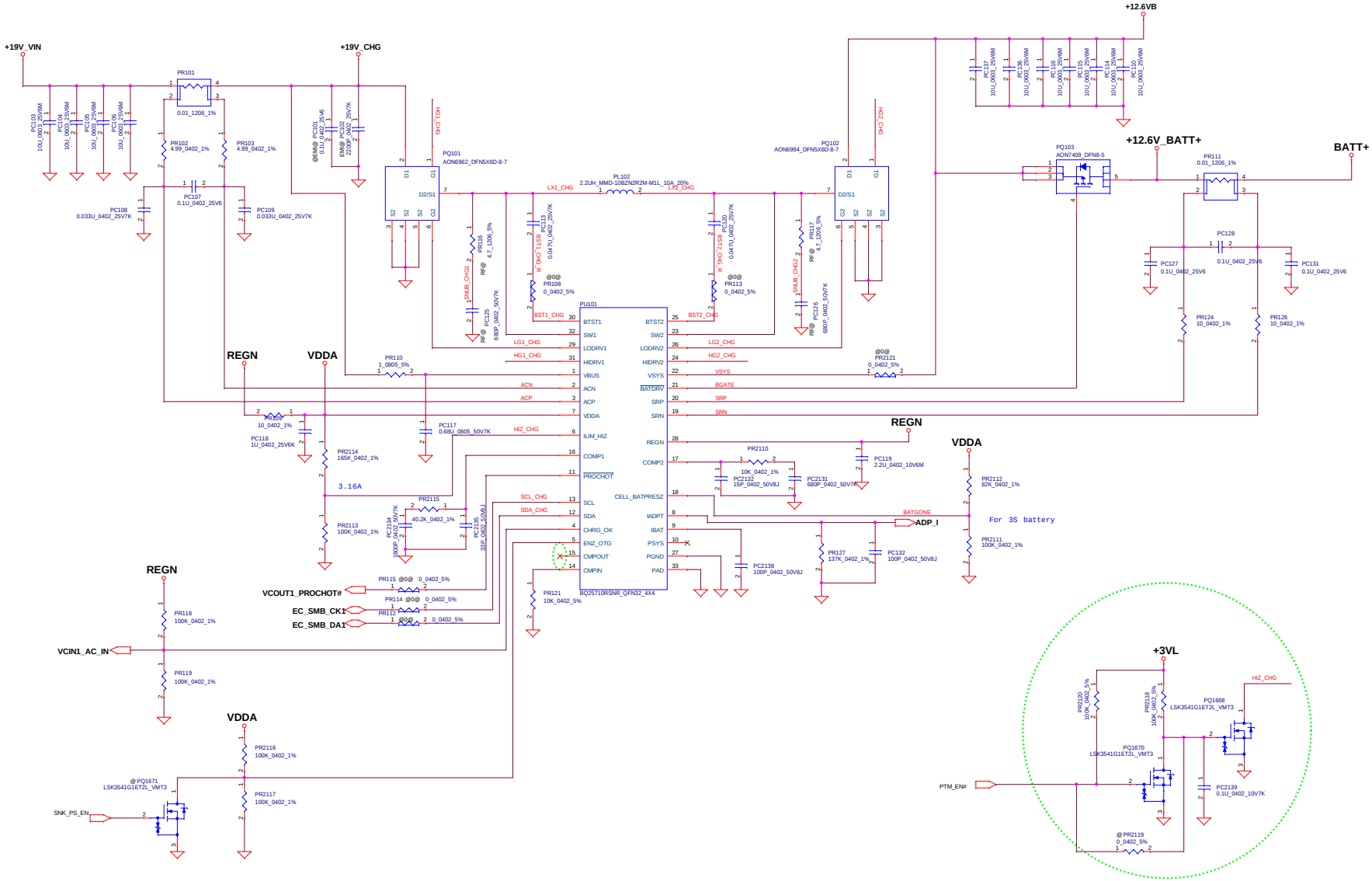

Security Classification	Compal Secret Data		
Issued Date	2018/04/25	Deciphered Date	2020/06/30

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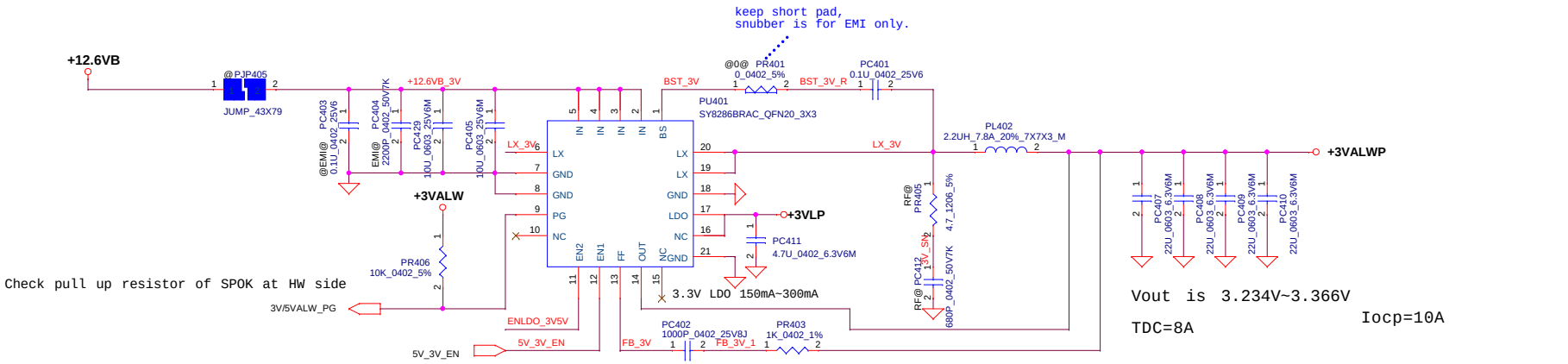
Compal Electronics, Inc.			
Title	PWR- CHARGER		
Size: Custom	Document Number: LA-H151P		Rev: 1.0
Date: Wednesday, January 02, 2019	Sheet 84 of 37		

Module model information

SY8288B_V5_single.mdd
SY8288B_V5_dual.mdd

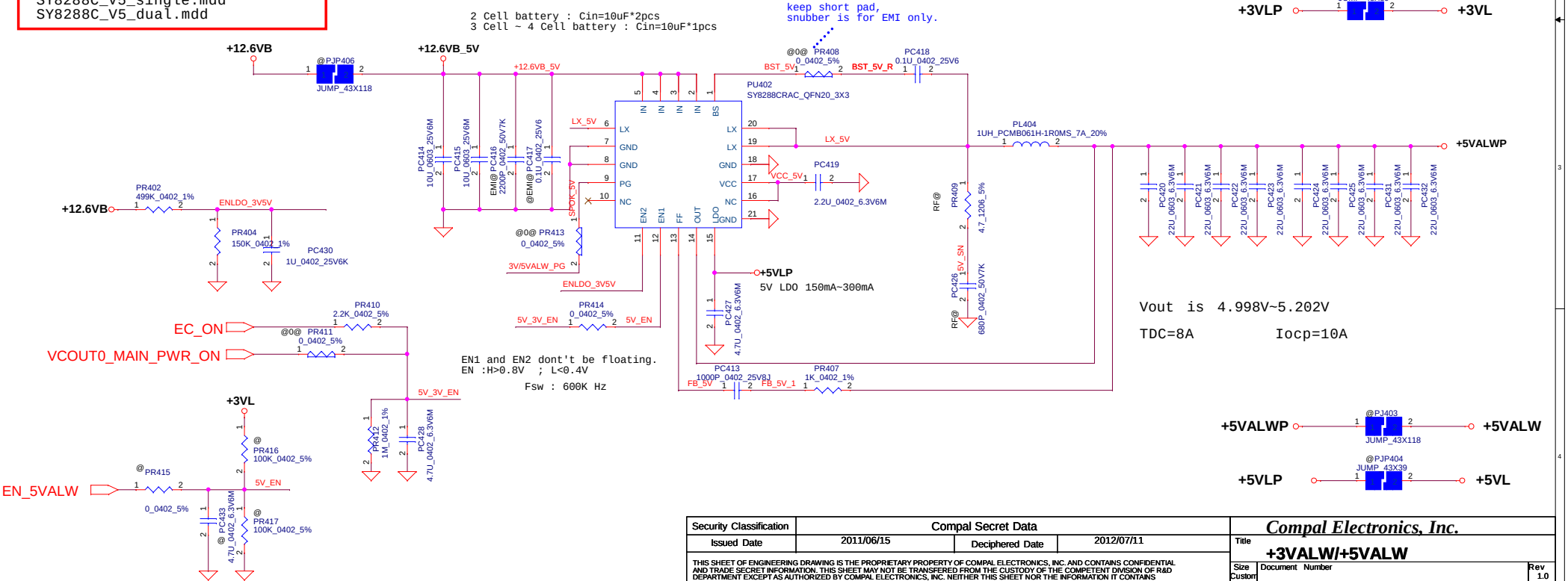


+3VALWP — @PJ401 JUMP_43X118 — +3VALW

+3VLP — @PJP402 JUMP_43X39 — +3VL

Module model information

SY8288C_V5_single.mdd
SY8288C_V5_dual.mdd



+5VALWP — @PJ403 JUMP_43X118 — +5VALW

+5VLP — @PJP404 JUMP_43X39 — +5VL

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: +3VALW/+5VALW

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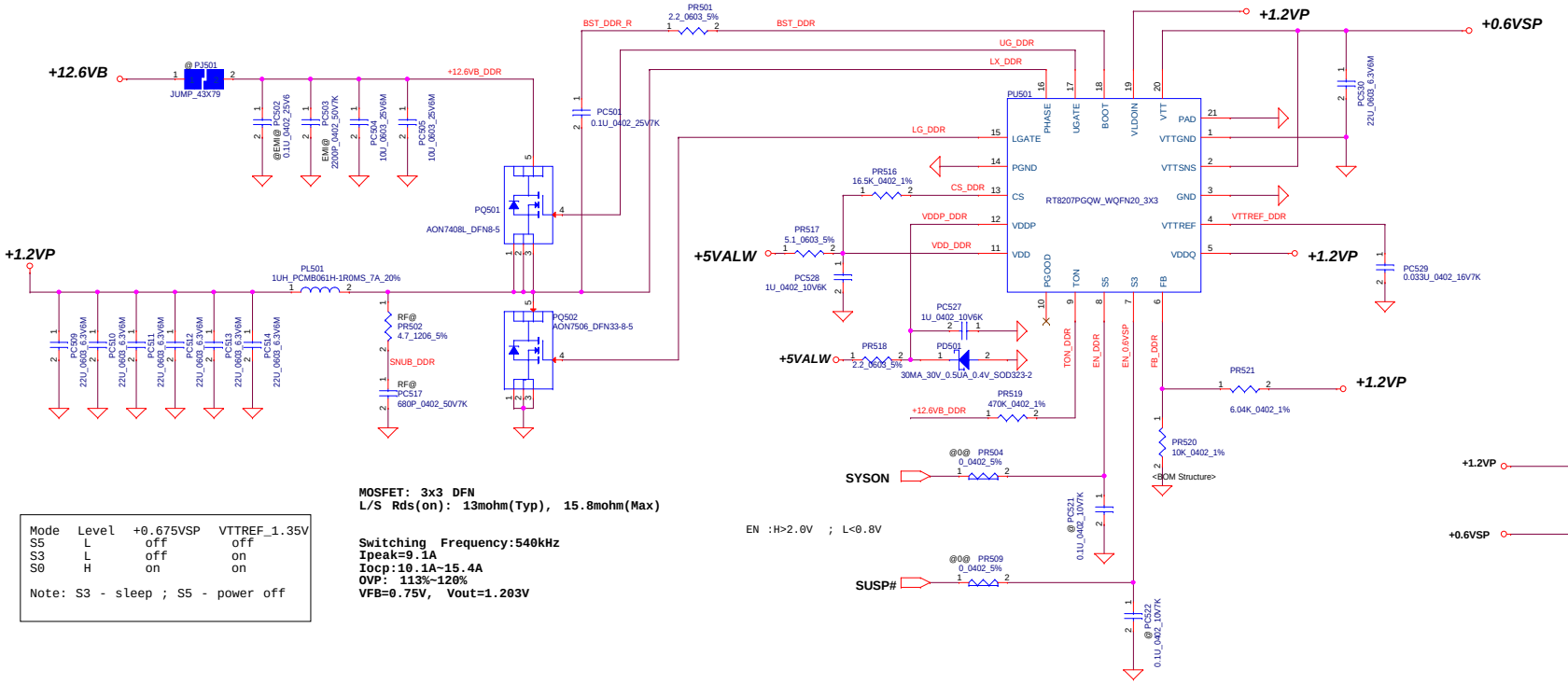
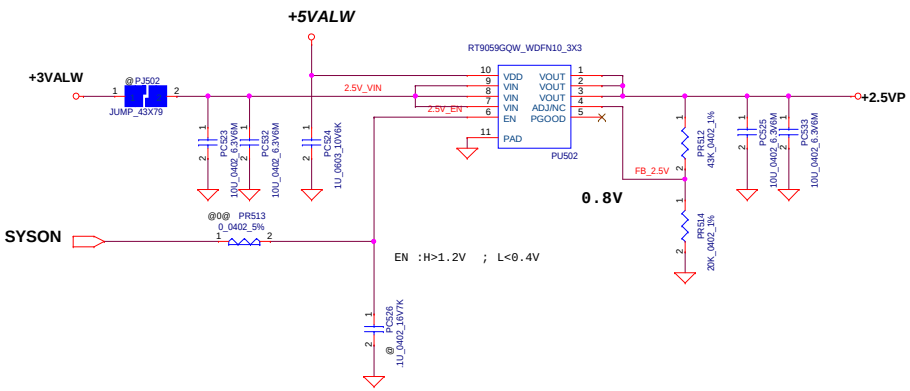
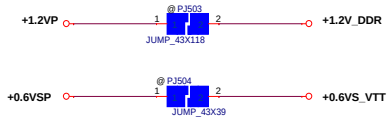
Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.



Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off





Security Classification	Compal Secret Data		
Issued Date	2017/03/09	Deciphered Date	2018/06/30

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Compal Electronics, Inc.

Title: PWR- 1.2VP/0.6VSP/2.5VP

Size	Document Number	Rev
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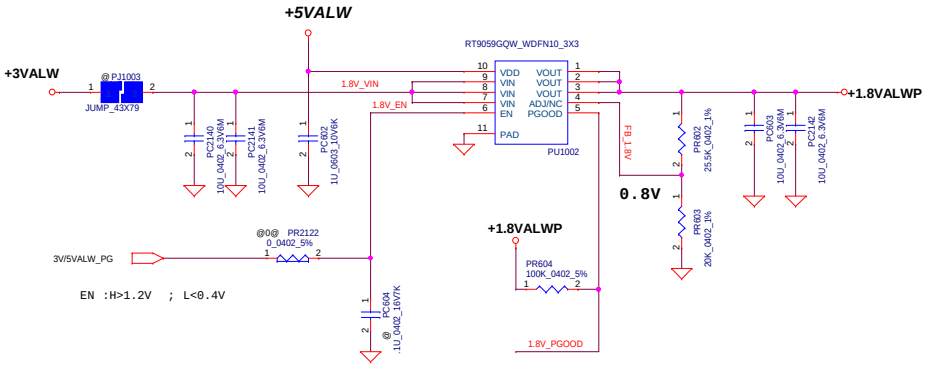

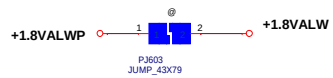

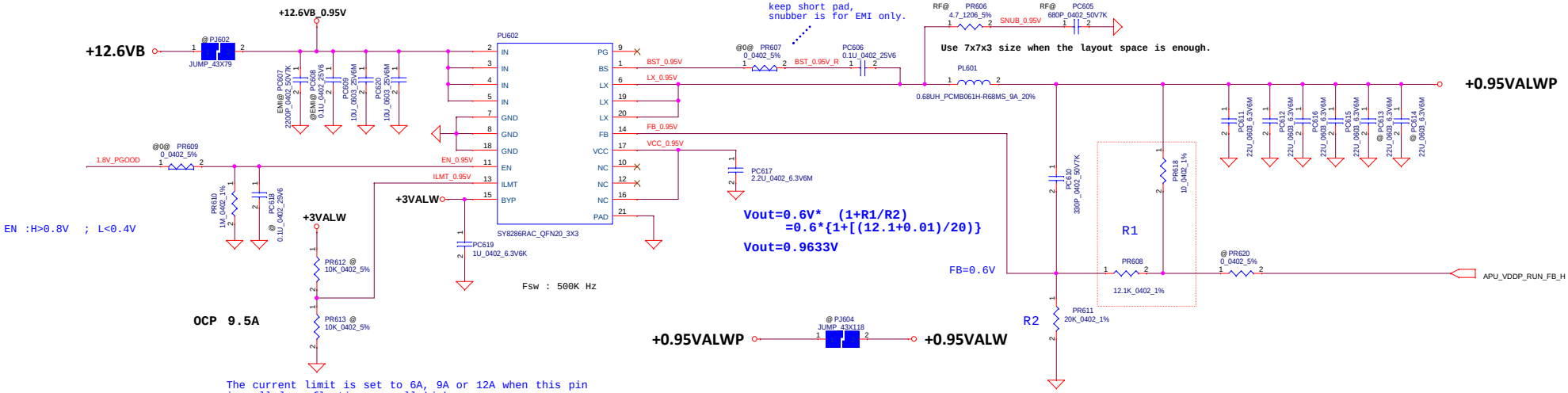

Security Classification	Compal Secret Data		
Issued Date	2017/03/09	Deciphered Date	2018/06/30

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Compal Electronics, Inc.

Title: **PWR- 1.8VALWP/1VALWP**

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Module model information

RT3661AB_V2A.mdd for IC portion

RT3661AB_V2B.mdd for SW portion

+12.6VB

APU_core
TDC 11A
Peak Current 15A
OCP current >21A
Load line 4mV/A
FSW=300kHz
DCR 4.3mohm +/-5%
TYP MAX
H/S Rds(on) :6.8mohm , 8.6mohm
L/S Rds(on) :2mohm , 2.5mohm

EN: High > 2V, Low < 0.8V
Can't be floating.

ISEN1P_APU to ISEN1N_APU must <40mV

Confirm HW side the pull high resistor

PR816, PR823 are for debug only,
APU_VDD_SEN, APU_VDD_RUN_FB_L need have 10ohm at HW size.

100 degree C
Close to PQ804

R2

Rp3

Rp4

PR812 is for debug only,
APU_VDDNB_SEN needs have 10ohm at HW size.

$$V_{TSEN_NB_ADC} = 80\mu A \cdot \left[\left(\frac{R_2 \cdot R_{NTC}}{R_2 + R_{NTC}}\right) + \left(\frac{R_{p3} \cdot R_{p4}}{R_{p3} + R_{p4}}\right)\right]$$

RT3661AB SET1, TSEN and TSEN_NB Pin Setting Function:
AI_VDD=100%, AI_VDDNB=100%
QR Threshold: Disable
Frequency: 300kHz
VDD and VDDNB Initial Offset: 0mV (PS0)
VDD and VDDNB PHOCP Setting Ratio: 150%

100 degree C
Close to PQ802

Rp1

R1

Rp2

APU_SVD and APU_SVC RC filter put CPU side.
APU_SVT RC filter put controller side.

$$V_{TSEN_ADC} = 80\mu A \cdot \left[\left(\frac{R_1 \cdot R_{NTC}}{R_1 + R_{NTC}}\right) + \left(\frac{R_{p1} \cdot R_{p2}}{R_{p1} + R_{p2}}\right)\right]$$

Close to PL801

Close to PL802

APU_CORE_NB
TDC 11A
Peak Current 15 A
OCP current > 21A
Load line 4mV/A
FSW=300kHz
DCR 4.3mohm +/-5%
TYP MAX
H/S Rds(on) :6.8mohm , 8.6mohm
L/S Rds(on) :2mohm , 2.5mohm

Security Classification	Compal Secret Data		
Issued Date	2018/01/08	Deciphered Date	2018/01/08

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Compal Electronics, Inc.			
Title	+APU_CORE/+APU_CORE_NB		
Size: Custom	Document Number: LA-H151P		Rev: 1.0
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Security Classification	Compal Secret Data		
Issued Date	2017/03/09	Deciphered Date	2018/06/30

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Compal Electronics, Inc.

Title: **BLANK**

Size: Custom | Document Number: **LA-H151P** | Rev: 1.0

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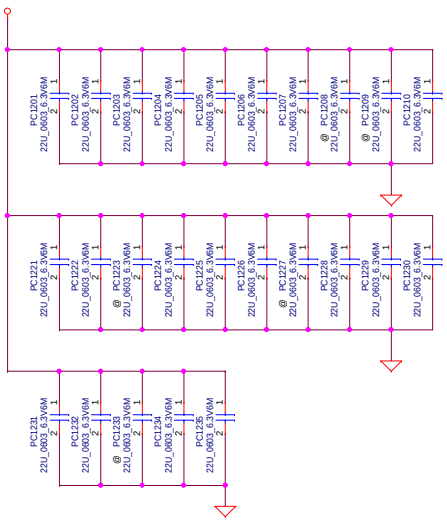
+APU_CORE

+APU_CORE

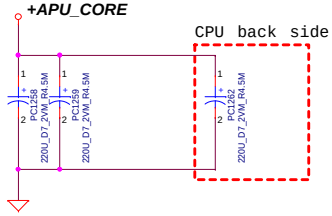


APU_CORE

220uF*3
22uF*20

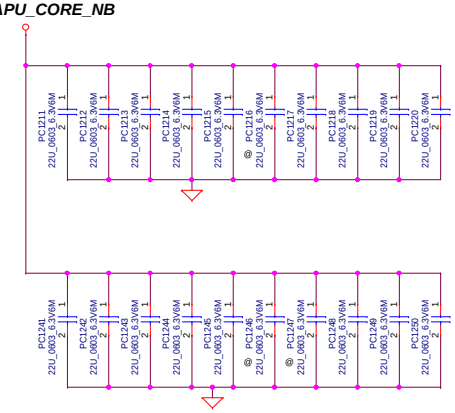
+APU_CORE

CPU_back_side

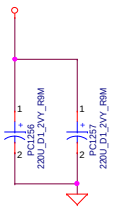


+APU_CORE_NB

+APU_CORE_NB



+APU_CORE_NB



APU_CORE_NB
220uF*2
22uF*17

Security Classification	Compal Secret Data		
Issued Date	2016/12/05	Deciphered Date	2017/12/05

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Compal Electronics, Inc.

Title: +APU_CORE Cap

Size	Document Number	Rev
C		1.0

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